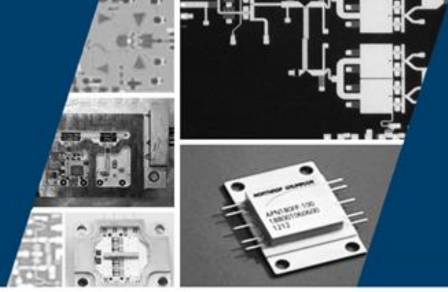
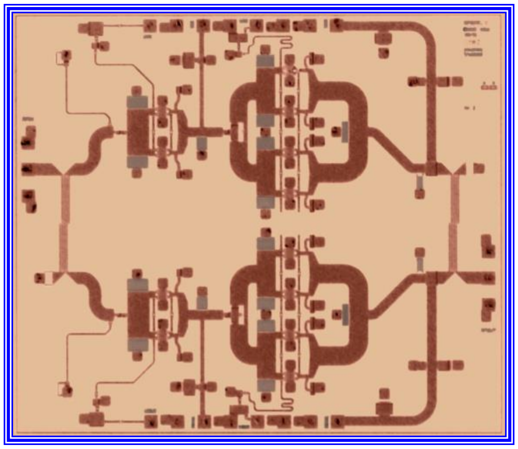
APN167
43-46 GHz
GaN Power Amplifier



NORTHROP GRUMMAN

Advance Datasheet

Revision: January 2015



X = 3.7mm Y = 3.2mm

Product Features

- RF frequency: 43 to 46 GHz
- Linear Gain: 20 dB typ.
- Psat: 39 dBm typ.
- PAE @ Psat: 20%
- Die Size: < 11.84 sq. mm.
- 0.2um GaN HEMT
- 4 mil substrate
- DC Power: 28 VDC @ 1008 mA

Applications

- Military SatCom
- Phased-Array Radar Applications
- Terminal Amplifiers

Product Description

The APN167 monolithic GaN HEMT amplifier is a broadband, two-stage power device, designed for use in Military SatCom and Radar Applications. To ensure rugged and reliable operation, HEMT devices are fully passivated. Both bond pad and backside metallization are Ti/Au, which is compatible with conventional die attach, thermocompression, and thermosonic wire bonding assembly techniques.

Performance Characteristics (Ta = 25°C)

Specification	Min	Typ	Max	Unit
Frequency	43		46	GHz
Linear Gain	18	20		dB
Input Return Loss	17	22		dB
Output Return Loss	17	25		dB
P1dB		35.5		dBm
Psat	38.5	39		dBm
PAE @ Psat		20		%
Vd1=Vd1a, Vd2=Vd2a		28		V
Vg1=Vg1a		-4.5		V
Vg2=Vg2a		-4.5		V
Id1+Id1a		336		mA
Id2+Id2a		672		mA

* Pulsed-Power On-Wafer

Absolute Maximum Ratings (Ta = 25°C)

Parameter	Min	Max	Unit
Vd1=Vg1a, Vd2=Vg2a	20	28	V
Id1+Id1a		336	mA
Id2+Id1a		672	mA
Vg1, Vg1a, Vg2, Vg2a	-5	0	V
Input drive level		TBD	dBm
Assy. Temperature (60 seconds)		300	deg. C

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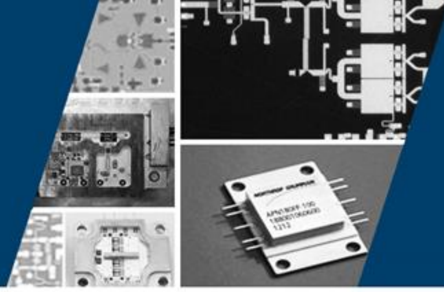
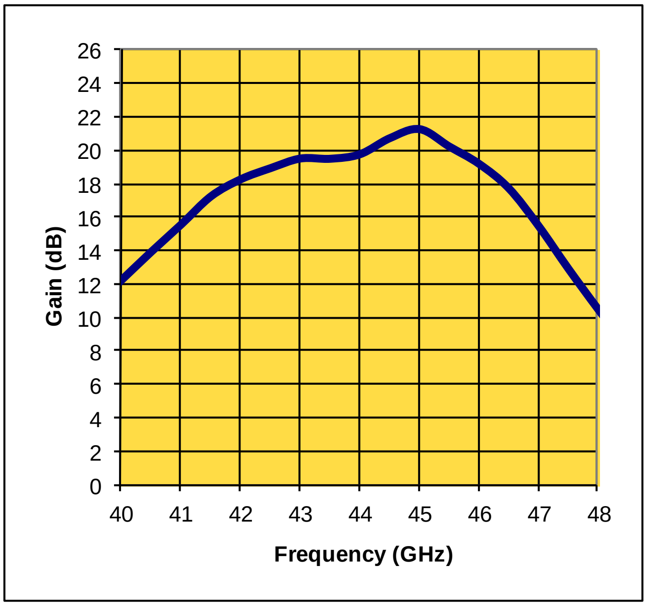


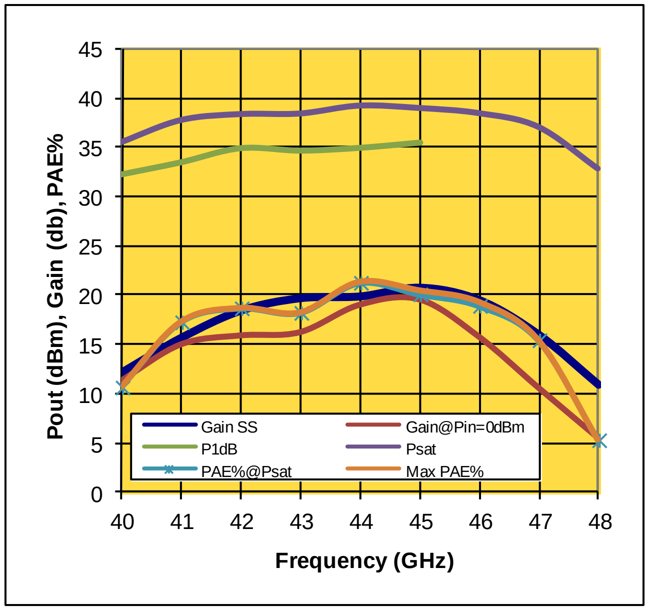
Measured Performance Characteristics (Typical Performance at 25°C)

Vd = 28.0 V, Id1+Id1a = 336 mA, Id2+Id2a = 672 mA

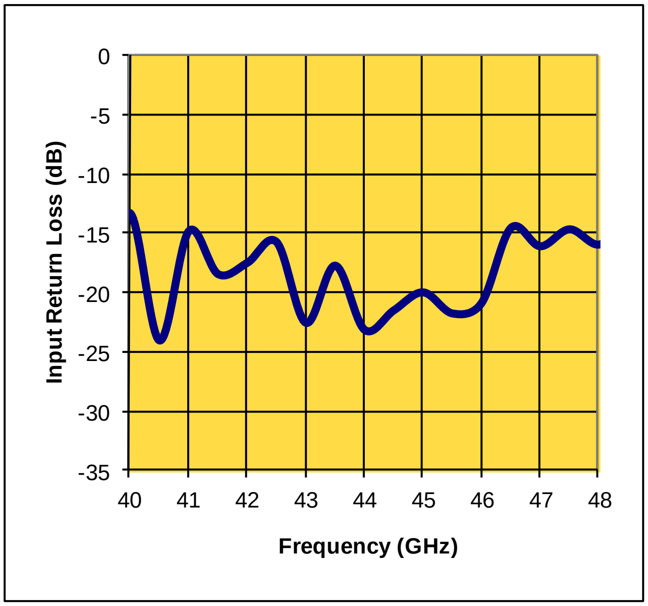
Linear Gain vs. Frequency



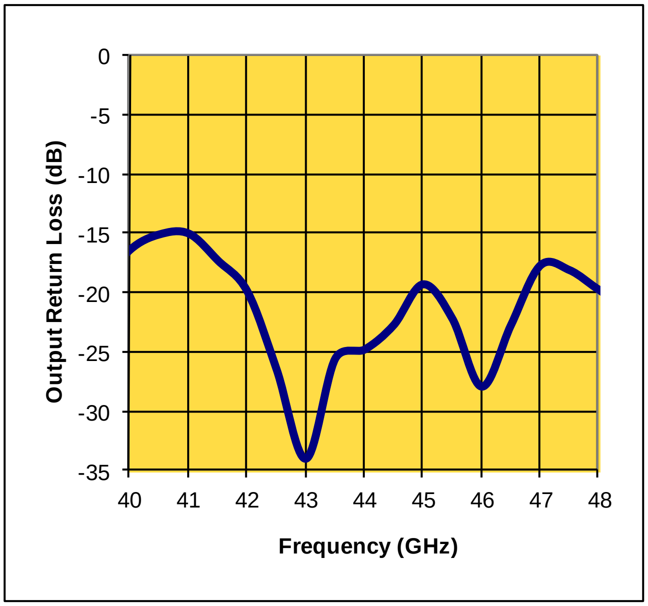
Power, Gain, PAE% vs. Frequency **



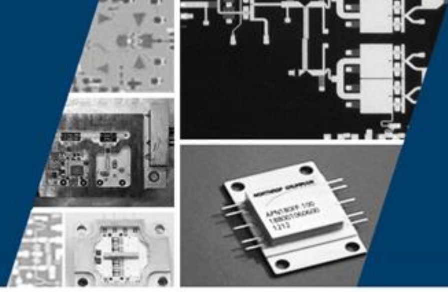
Input Return Loss vs. Frequency



Output Return Loss vs. Frequency

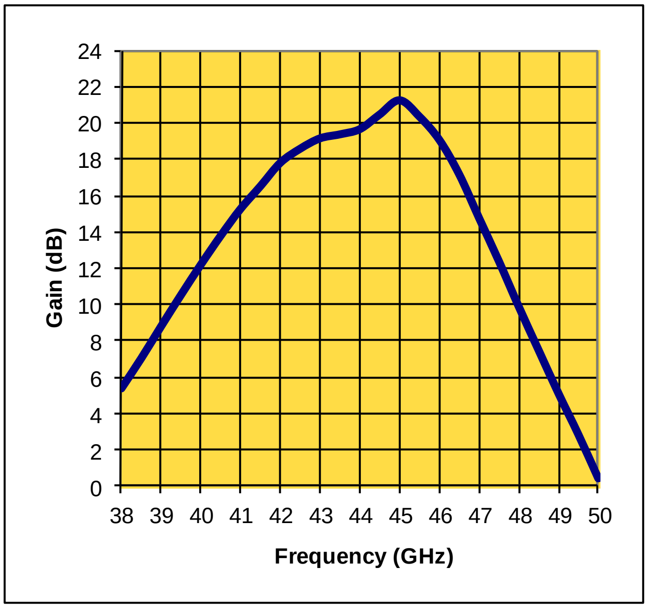


* Pulsed-Power On-Wafer , ** CW Fixtured

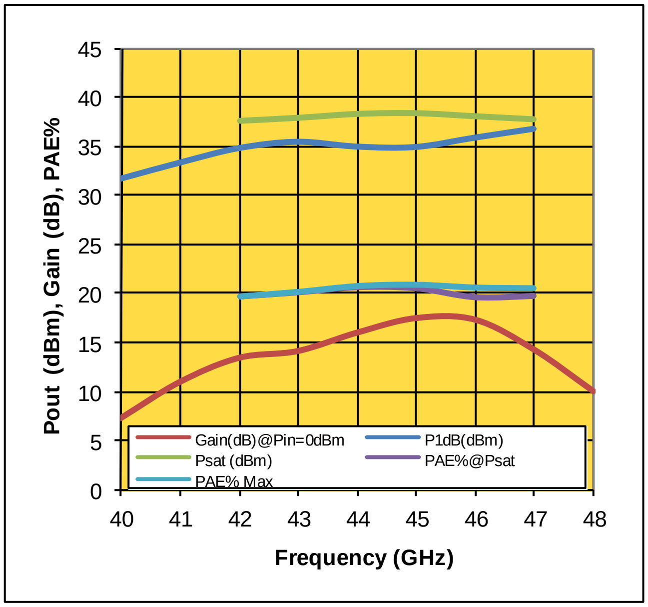


Measured Performance Characteristics (Typical Performance at 25°C)
Vd = 24.0 V, Id1+Id1a = 336 mA, Id2+Id2a = 672 mA *

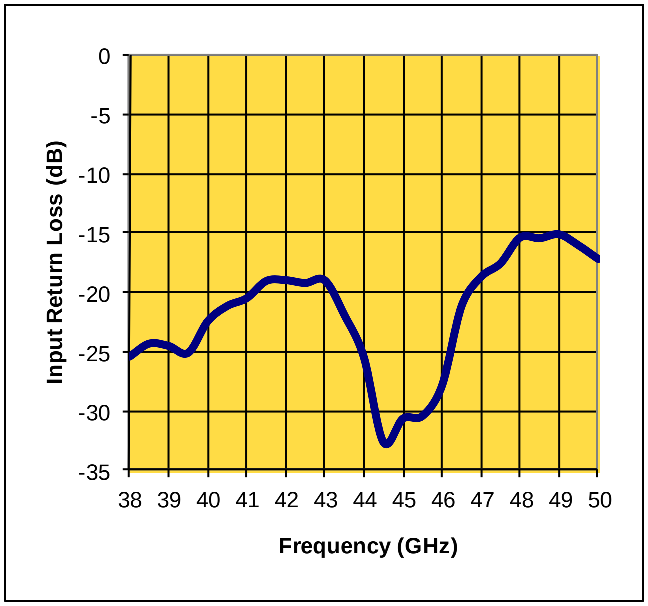
Linear Gain vs. Frequency



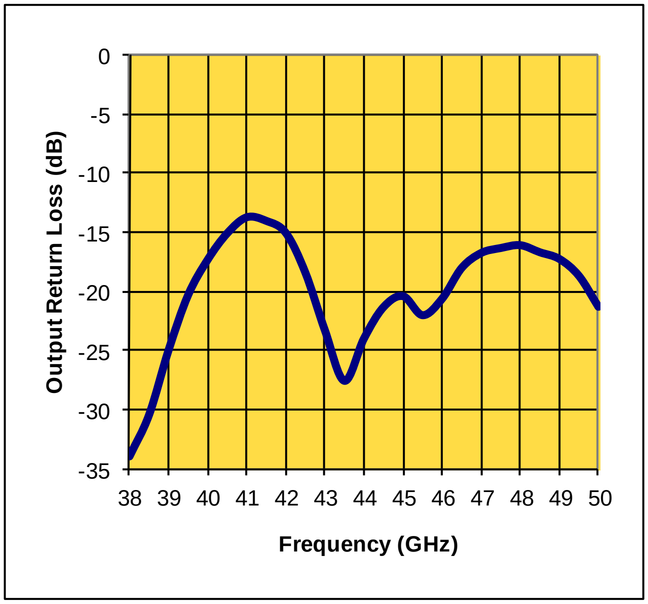
Power, Gain, PAE% vs. Frequency



Input Return Loss vs. Frequency



Output Return Loss vs. Frequency



* Pulsed-Power On-Wafer

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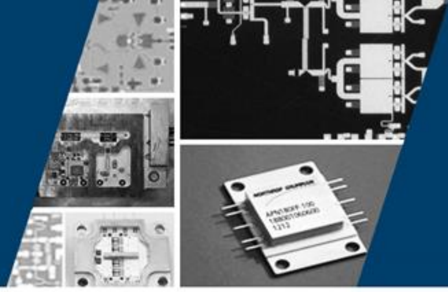
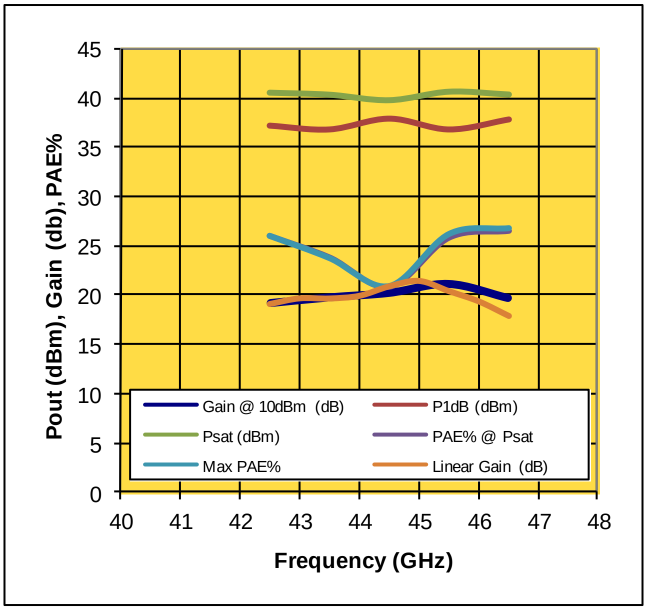


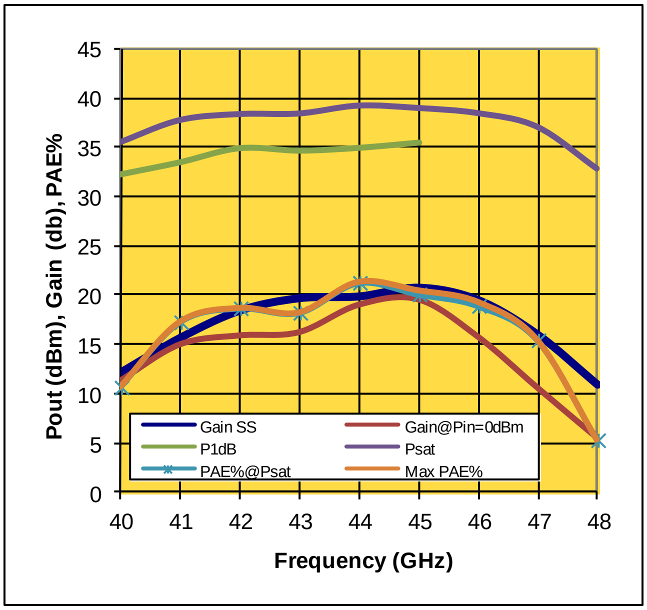
Measured Performance Characteristics (Typical Performance at 25°C)

Vd = 28.0 V, Id1+Id1a = 336 mA, Id2+Id2a = 672 mA

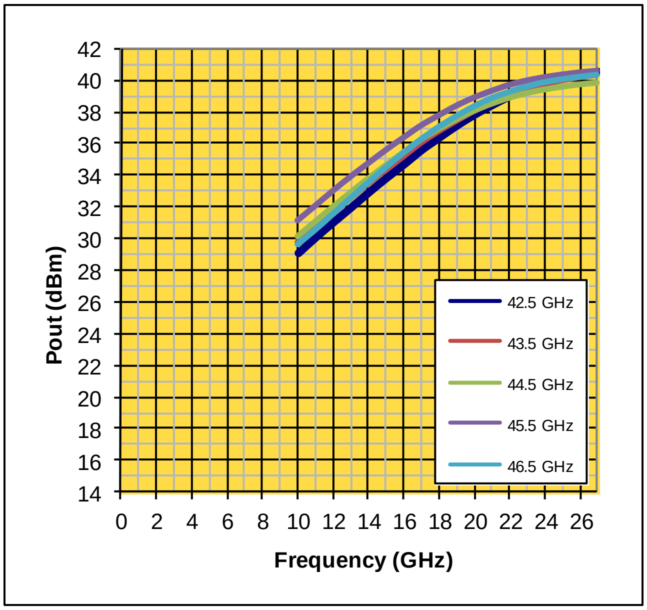
Power, Gain, PAE% vs. Frequency *



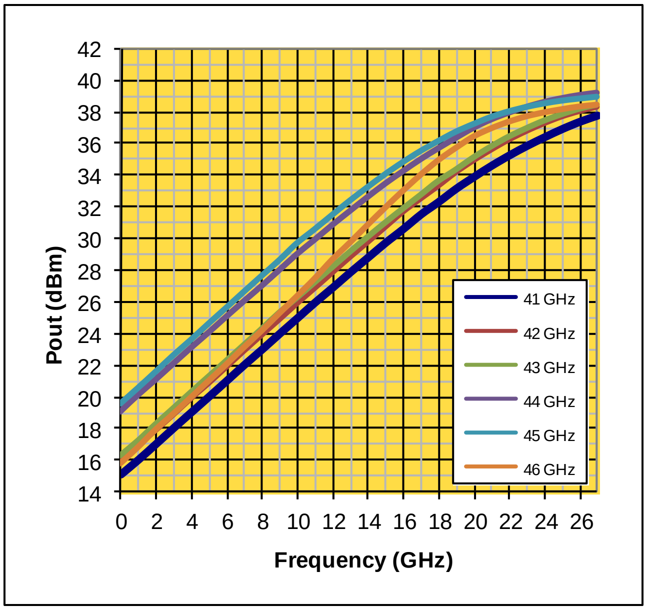
Power, Gain, PAE% vs. Frequency **



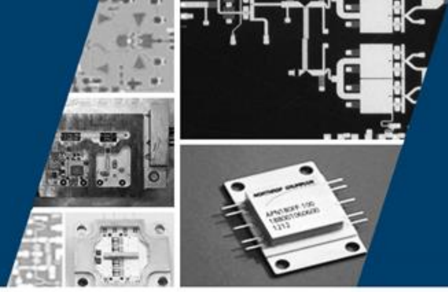
Output Power vs. Input Power *



Output Power vs. Input Power **

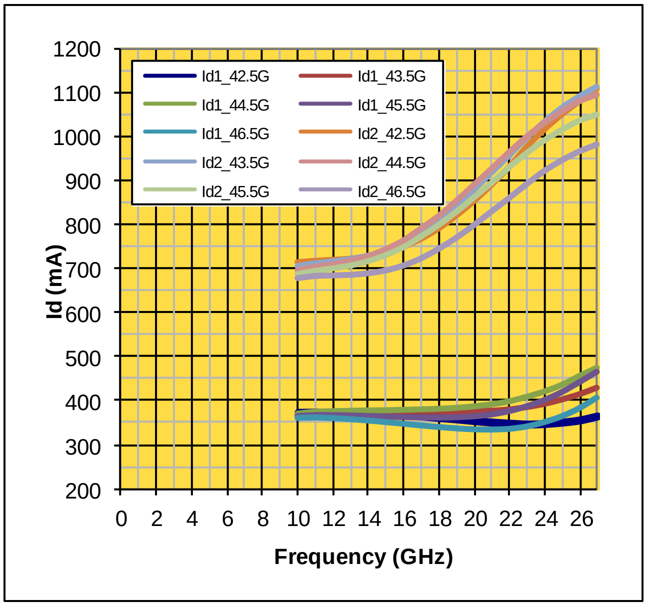


* Pulse-Power On-Wafer, ** CW Fixtured

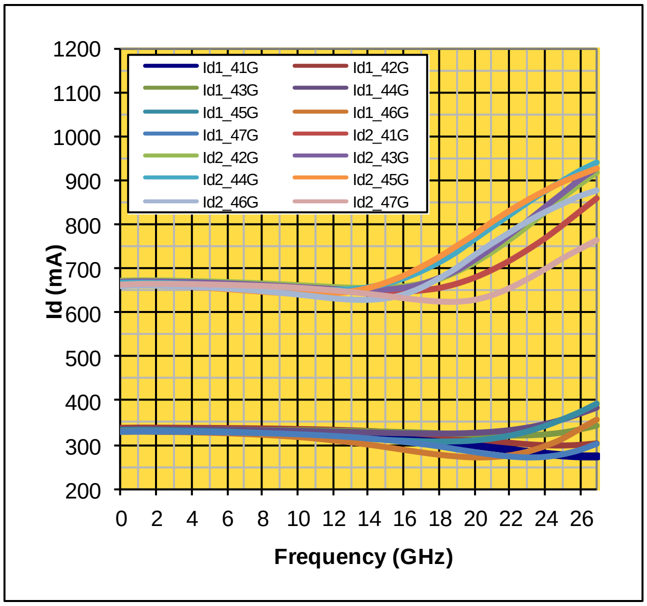


Measured Performance Characteristics (Typical Performance at 25°C)
Vd = 28.0 V, Id1+Id1a = 336 mA, Id2+Id2a = 672 mA

Power, Gain, PAE% vs. Frequency *



Power, Gain, PAE% vs. Frequency **



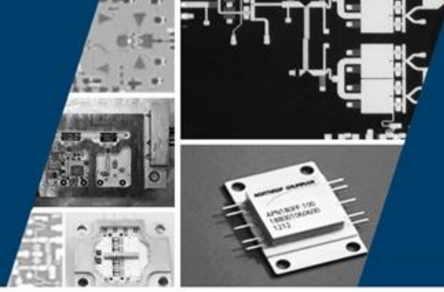
* Pulse-Power On-Wafer, **CW Fixtured

Thermal Properties

Preliminary Thermal Properties with die mounted with 1mil 80/20 AuSn Eutectic to 25mil CuW Shim.

Conditions	Shim Boundary Temperature	Junction Temperature Tjc	Thermal Resistance θjc
Vd = 28V, Id1+Id1a = 368 mA * Id2 + Id2a = 921 mA * Pin=25.95 dBm Pout=39.08 dBm	25 ºC 49.6 ºC	162.8 ºC 200.0 ºC **	4.9 ºC/W 5.3 ºC/W

* Vd = 28.0 V, Idq1+Id1aq = 336 mA, Id2q+Id2aq = 672 mA
** Max recommended. Pre-qualification reliability testing indicates that MTTF in excess of 10^5 hours can be achieved by ensuring Tjc is kept below 200ºC.



Measured Performance Characteristics (Typical Performance at 25°C)
Vd = 28.0 V, Id1+Id1a = 336 mA, Id2+Id2a = 672 mA *

Freq GHz	S11 Mag	S11 Ang	S21 Mag	S21 Ang	S12 Mag	S12 Ang	S22 Mag	S22 Ang
34.0	0.110	-101.841	0.484	-122.815	0.003	76.615	0.117	1.410
34.5	0.096	-115.160	0.564	-138.227	0.003	27.194	0.097	-23.379
35.0	0.071	-126.967	0.657	-153.903	0.002	19.337	0.080	-45.269
35.5	0.055	-148.663	0.762	-169.695	0.002	65.428	0.057	-63.815
36.0	0.059	17.195	0.887	174.835	0.002	28.841	0.041	-85.852
36.5	0.049	66.150	1.032	158.855	0.003	49.684	0.025	-133.162
37.0	0.044	87.520	1.210	143.065	0.003	21.637	0.020	20.382
37.5	0.046	111.189	1.429	127.274	0.004	34.005	0.015	43.110
38.0	0.054	77.822	1.710	110.887	0.004	38.903	0.013	51.419
38.5	0.060	70.129	2.073	93.604	0.006	14.638	0.019	41.519
39.0	0.059	54.528	2.547	75.429	0.007	16.914	0.045	97.535
39.5	0.057	40.942	3.125	55.173	0.008	-5.825	0.086	143.408
40.0	0.075	36.181	3.831	33.623	0.008	-17.491	0.130	118.876
40.5	0.083	30.121	4.657	10.409	0.009	-45.099	0.178	92.759
41.0	0.087	30.891	5.599	-14.815	0.009	-66.837	0.220	62.945
41.5	0.105	22.066	6.537	-40.073	0.010	-93.443	0.226	35.064
42.0	0.110	4.235	7.690	-67.989	0.010	-112.892	0.212	3.391
42.5	0.115	-7.029	8.540	-97.870	0.011	-138.365	0.157	-26.472
43.0	0.123	-23.958	9.177	-127.764	0.011	-70.641	0.087	-46.456
43.5	0.091	-41.380	9.317	-156.756	0.011	74.750	0.039	-48.488
44.0	0.067	-47.232	9.458	111.449	0.013	136.755	0.045	-4.377
44.5	0.040	-78.825	10.192	150.906	0.011	119.834	0.065	-17.427
45.0	0.020	-6.900	11.289	117.318	0.011	86.296	0.073	-61.977
45.5	0.019	-6.146	10.787	81.440	0.016	52.268	0.054	-117.204
46.0	0.041	53.231	10.014	47.229	0.012	18.448	0.065	-16.450
46.5	0.078	78.114	8.660	11.820	0.013	-4.884	0.107	134.470
47.0	0.107	56.365	6.802	-21.376	0.010	-60.602	0.135	99.370
47.5	0.129	37.462	5.201	-50.756	0.007	-94.563	0.146	74.003
48.0	0.171	15.729	3.870	-76.996	0.008	-78.311	0.154	54.560
48.5	0.175	-1.411	2.886	-100.020	0.006	-35.341	0.146	38.277
49.0	0.182	-12.623	2.168	-120.840	0.008	41.826	0.139	14.877
49.5	0.166	-26.498	1.642	-141.538	0.011	35.637	0.115	2.399
50.0	0.143	-38.350	1.233	-158.589	0.004	67.183	0.084	-2.484

* Pulsed-Power On-Wafer

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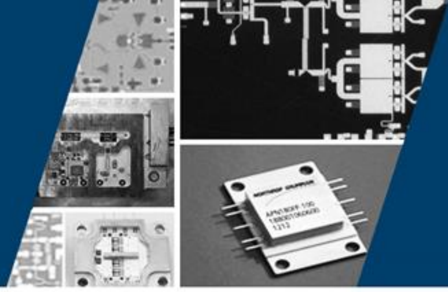
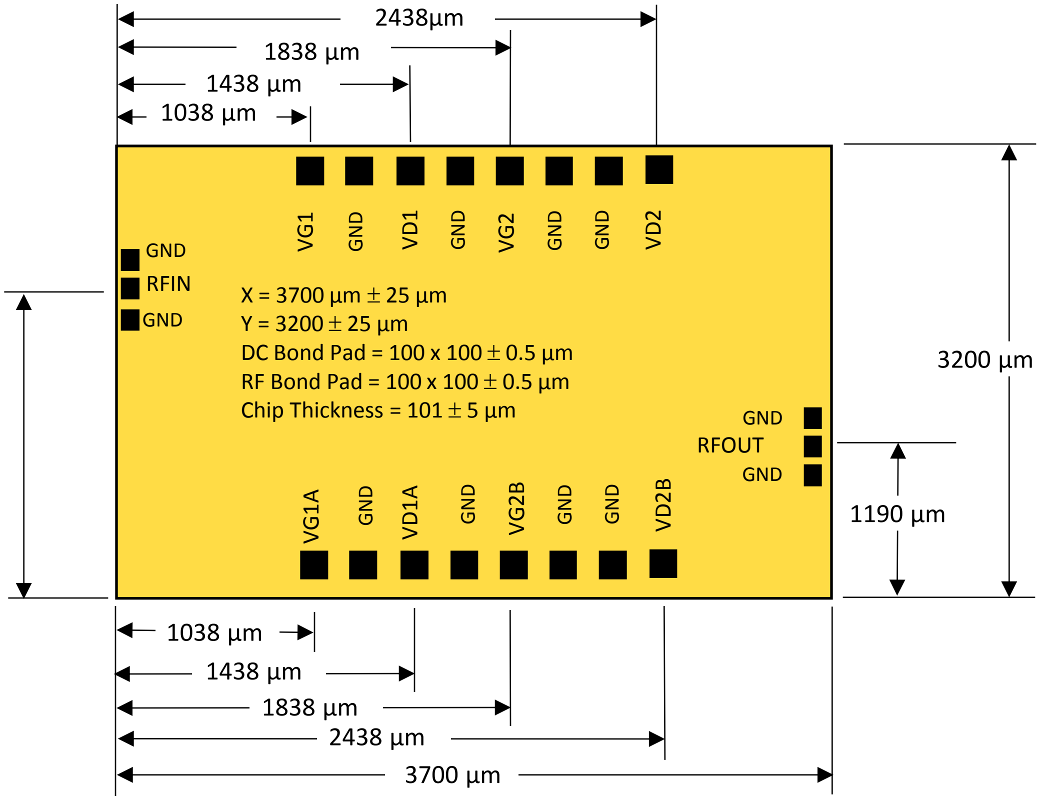


Die Size and Bond Pad Locations (Not to Scale)

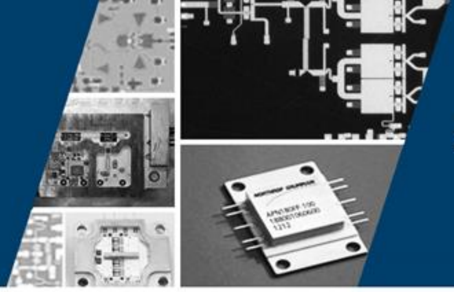


Biasing/De-Biasing Details:

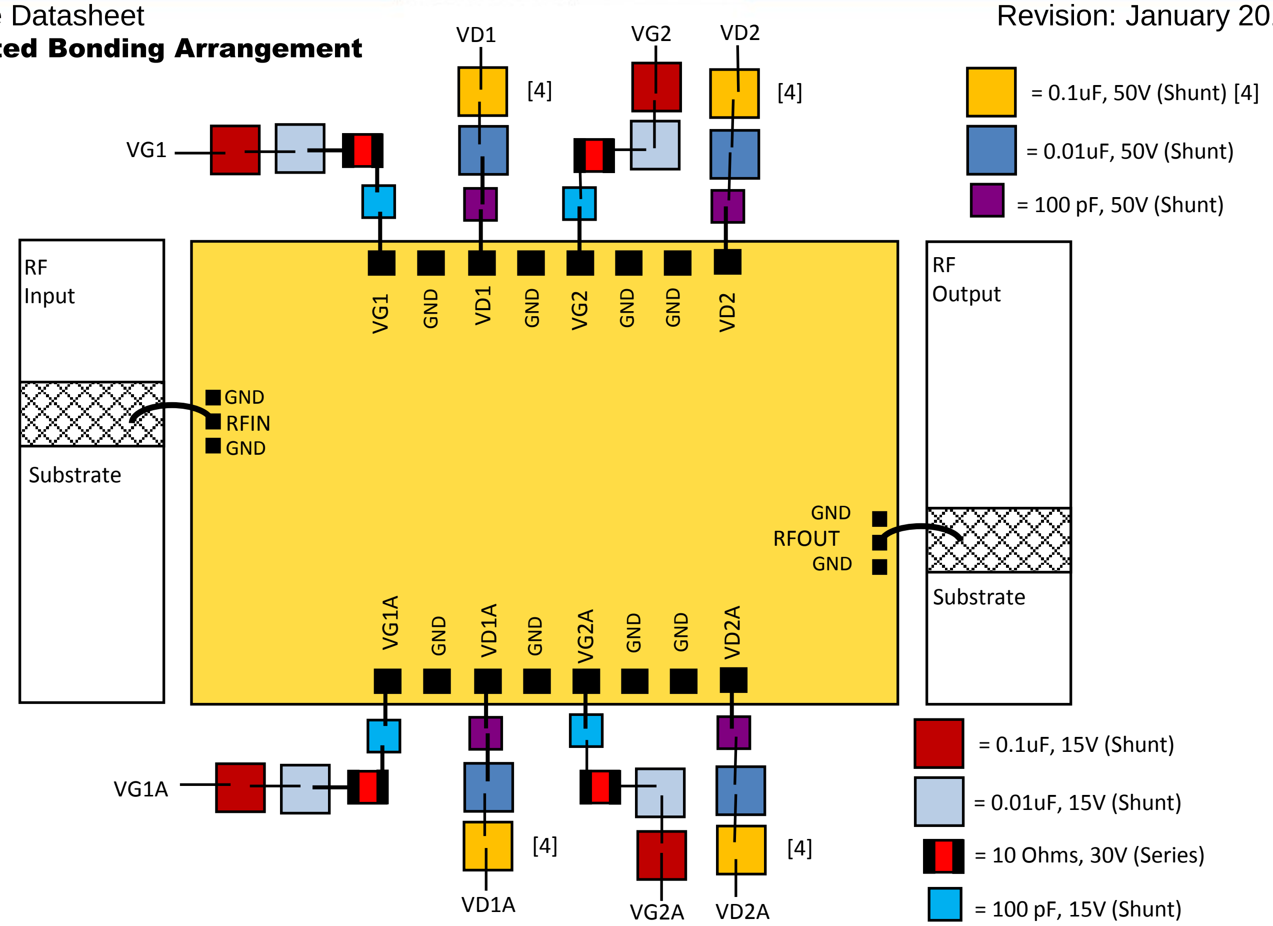
Bias for 1st stage is from top. The 2nd stages must bias up from both sides.

Listed below are some guidelines for GaN device testing and wire bonding:

a. Limit positive gate bias (G-S or G-D) to < 1V
b. Know your devices' breakdown voltages
c. Use a power supply with both voltage and current limit.
d. With the power supply off and the voltage and current levels at minimum, attach the ground lead to your test fixture.
    i. Apply negative gate voltage (-5 V) to ensure that all devices are off
    ii. Ramp up drain bias to ~10 V
    iii. Gradually increase gate bias voltage while monitoring drain current until 20% of the operating current is achieved
    iv. Ramp up drain to operating bias
    v. Gradually increase gate bias voltage while monitoring drain current until the operating current is achieved
e. To safely de-bias GaN devices, start by debiasing output amplifier stages first (if applicable):
    i. Gradually decrease drain bias to 0 V.
    ii. Gradually decrease gate bias to 0 V.
    iii. Turn off supply voltages
f. Repeat de-bias procedure for each amplifier stage



Suggested Bonding Arrangement



Recommended Assembly Notes

1. Bypass caps should be 100 pF (approximately) ceramic (single-layer) placed no farther than 30 mils from the amplifier.
2. Best performance obtained from use of <10 mil (long) by 3 by 0.5 mil ribbons on input and output.
3. Part must be biased from both sides as indicated.
4. The 0.1uF, 50V capacitors are not needed if the drain supply line is clean. If Drain Pulsing of the device is to be used, do **NOT** use the 0.1uF , 50V Capacitors.

Mounting Processes

Most NGAS GaN IC chips have a gold backing and can be mounted successfully using either a conductive epoxy or AuSn attachment. NGAS recommends the use of AuSn for high power devices to provide a good thermal path and a good RF path to ground. Maximum recommended temp during die attach is 320ºC for 30 seconds.

Note: Many of the NGAS parts do incorporate airbridges, so caution should be used when determining the pick up tool.

CAUTION: THE IMPROPER USE OF AuSn ATTACHMENT CAN CATASTROPHICALLY DAMAGE GaN CHIPS.

PLEASE ALSO REFER TO OUR "GaN Chip Handling Application Note" BEFORE HANDLING, ASSEMBLING OR BIASING THESE MMICS!

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