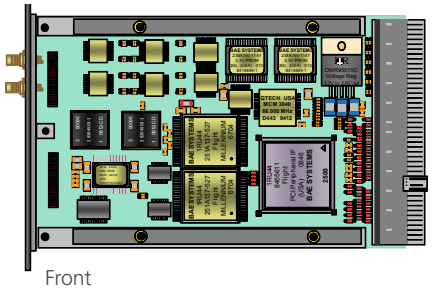
BAE SYSTEMS
INSPIRED WORK

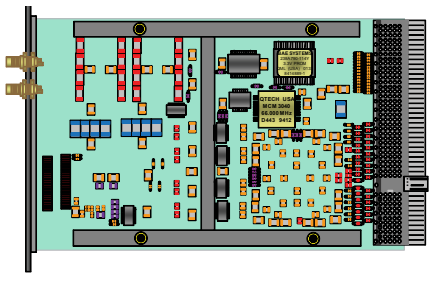
3U-160 CompactPCI® MIL-STD-1553B interface board

The 3U-160 CompactPCI MIL-STD-1553B board, available in engineering and flight versions, employs a BAE Systems radiation-hardened peripheral ASIC. The ASIC provides the MIL-STD-1553 bus interface function as well as access to on-board memory and the CompactPCI backplane.

The board contains one full-duplex flight UART with either RS-422 or LVDS signaling levels intended for use with devices, such as uplink receivers, downlink transmitters, asynchronous interfaces, cross-link devices, and payload electronics.



Front



Back

The MIL-STD-1553 board can operate alone or integrate with host processors, such as the RAD750® single board computer.A 32-bit embedded microcontroller with supporting Start-up ROM (SUROM) and SRAM may be used stand-alone, as a system I/O controller, or as a command pre-processor. In addition to the base software accompanying the board, BAE Systems offers additional software for the embedded microcontroller built into the ASIC.

The board provides redundant direct coupled or transformer coupled MIL-STD-1553 channels and can be set up as either a Bus Controller (BC) or Remote Terminal (RT). In addition to the 1553 interface, one full-duplex parallel port with input and output FIFO is provided at the CompactPCI backplane connector along with programmable discretes. Additional discretes are provided at the front panel.

The CompactPCI interface employs Hypertronics connectors. With minor limitations, it is compatible with 64-bit CompactPCI backplanes. The PCI interface is also capable of acting as the PCI central resource.

Specifications

Form factor
CompactPCI 3U (100 mm by 160 mm)
Weight: 500 grams (TBR)
Temperature range
-55 to +70 degrees Celsius (TBR)
Radiation hardness
Total dose: > 100 Krads (Si)
SEU: <4e-4 errors/card-day with 4 MB SRAM
Latchup: immune
Power dissipation
< 4 to 5 W typical
Power supply
3.3V ± 10 percent
2.5V generated via on-board regulator
Interface performance
32-bit, 33 MHz PCI bus – 132 MB/s burst
1553 – 1 MB/s burst
FIFO 40 MB/s burst full duplex memory
Memory (selectable)
Error corrected start-up memory (256 KB EEPROM or 64 KB PROM)
Error corrected SRAM (4 MB)
Software features
C Compiler, assembler, linker, and simulator available for embedded microcontroller
Example start-up ROM and VxWorks board support package provided
Green Hills Software's INTEGRITY real-time operating system can serve as alternate board-support package
Hardware reference manual and software users guide provided

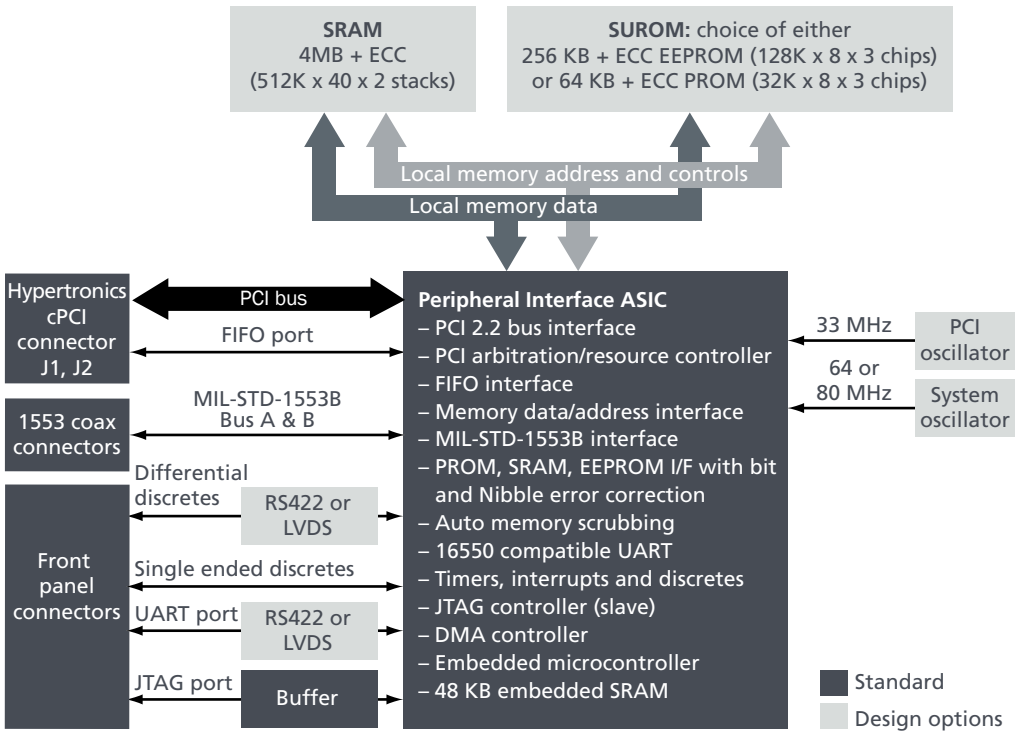
Configuration flexibility

There are thirteen single-ended +3.3V CMOS discretes, configurable as inputs or outputs, provided at the cPCI backplane connector and two more provided at the front panel connector.

Sixteen differential discretes are provided at the front panel connector. LVDS or RS-422 signaling levels can be selected at build in any combination in groups of four. For example, a design may have twelve LVDS input discretes and four RS-422 output discretes, or eight LVDS output discretes and eight RS-422 input discretes, etc.

A separate PCI oscillator may be included for use when the system clock frequency is not an integer multiple of the PCI bus frequency.

Hardware block diagram



Product ordering information

8451580-ZZZZZZZZ ← UART signaling levels: L = LVDS; R = RS-422

- SRAM volatile memory (error corrected): 4 = 4 MB; X = unpopulated
- SUROM non-volatile memory (error-corrected): E=256 KB EEPROM; P=64 KB PROM; X=unpopulated
- # of SpaceWire ports provided: 2 or 4
- SpaceWire oscillator: 5 = 50 MHz; X=unpopulated
- PCI oscillator: 3 = 33 MHz; X = unpopulated
- System oscillator: 6 = 66 MHz; 8 = 80 MHz (future)
- Version: E = engineering; F = flight

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