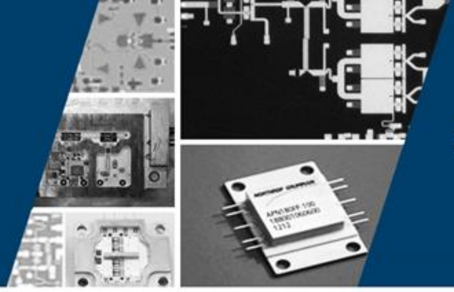
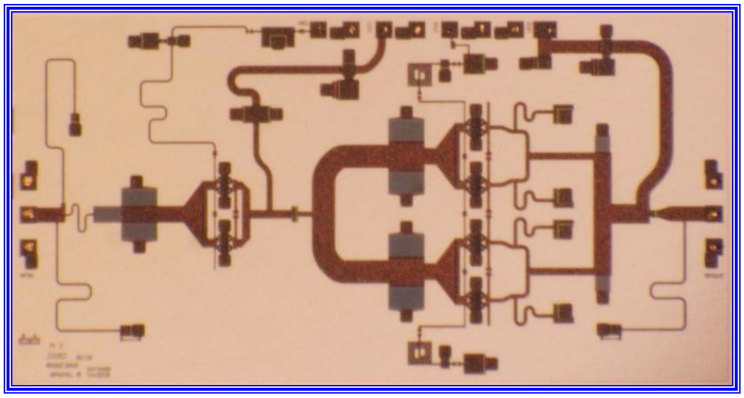
APN149
18-23 GHz
GaN Power Amplifier



NORTHROP GRUMMAN

Advance Datasheet

Revision: January 2015



X = 4.4mm Y = 2.28mm

Product Features

- RF frequency: 18 to 23 GHz
- Linear Gain: 20 dB typ.
- Psat: 38 dBm typ.
- Efficiency @ P3dB > 30 %
- Die Size: < 10.032 sq. mm.
- 0.2um GaN HEMT
- 4 mil SiC substrate
- DC Power: 28 VDC @ 544 mA

Performance Characteristics (Ta = 25°C)

Specification	Min	Typ	Max	Unit
Frequency	18		23	GHz
Linear Gain	19	23		dB
Input Return Loss	4	11		dB
Output Return Loss	6	11		dB
P1db		36		dBm
Psat	37.5	38.5		dBm
PAE @ Psat		30		%
Vd1, Vd2		28		V
Vg1		-3.5		V
Vg2		-3.5		V
Id1		144		mA
Id2		400		mA

Applications

- Military SatCom
- Phased-Array Radar Applications
- Point-to-Point Radio
- Point-to-Multipoint Communications
- Terminal Amplifiers

Product Description

The APN149 monolithic GaN HEMT amplifier is a broadband, two-stage power device, designed for use in Point-to-Point and Multipoint Digital Radios, Military SatCom and Radar Applications. To ensure rugged and reliable operation, HEMT devices are fully passivated. Both bond pad and backside metallization are Au-based that is compatible with epoxy and eutectic die attach methods.

Absolute Maximum Ratings (Ta = 25°C)

Parameter	Min	Max	Unit
Vd1, Vd2	20	28	V
Id1		144	mA
Id2+Id2a		400	mA
Vg1, Vg2	-5	0	V
Input drive level		TBD	dBm
Assy. Temperature (TBD seconds)		300	deg. C

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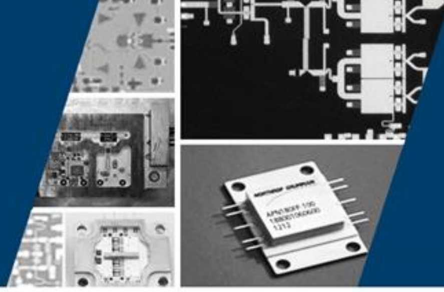
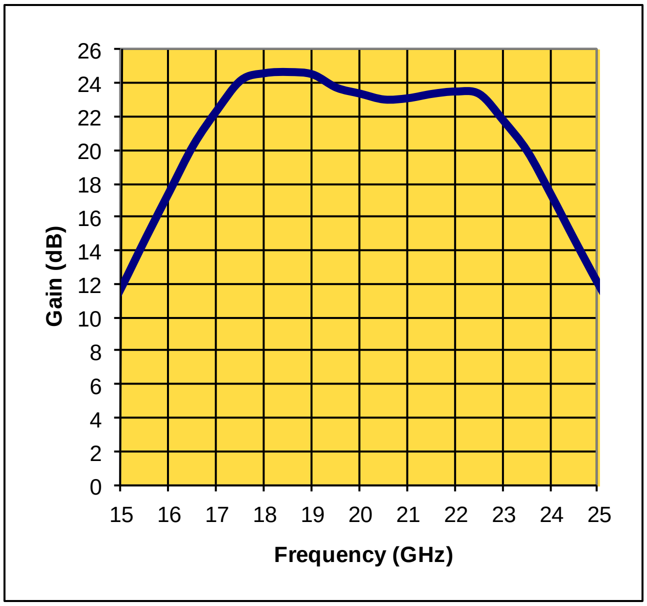
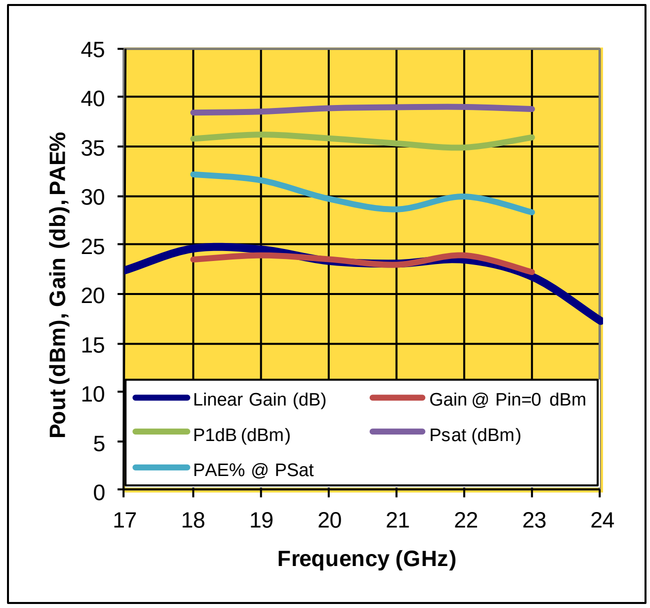


Measured Performance Characteristics (Typical Performance at 25°C)
Vd = 28.0 V, Id1 = 144 mA, Id2 = 400 mA *

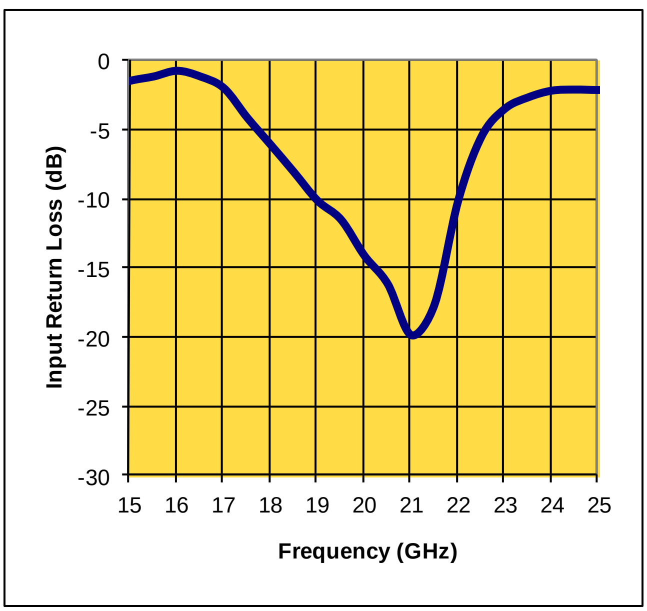
Linear Gain vs. Frequency



Power, Gain, PAE% vs. Frequency



Input Return Loss vs. Frequency



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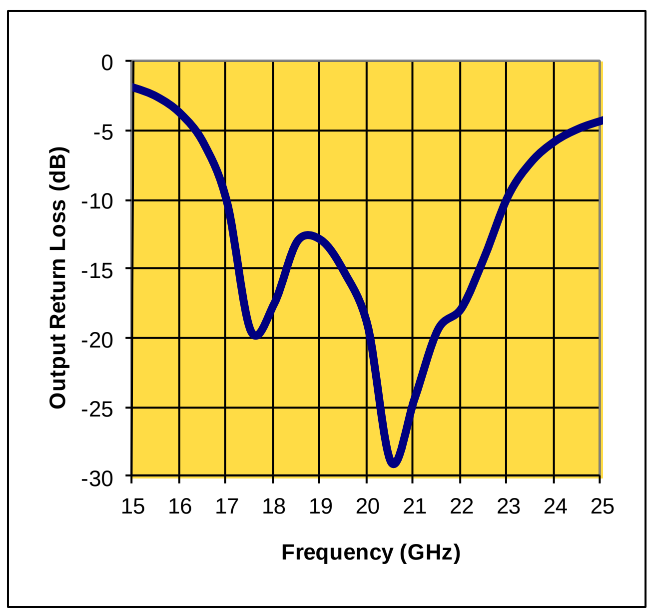

* Pulsed-Power On-Wafer

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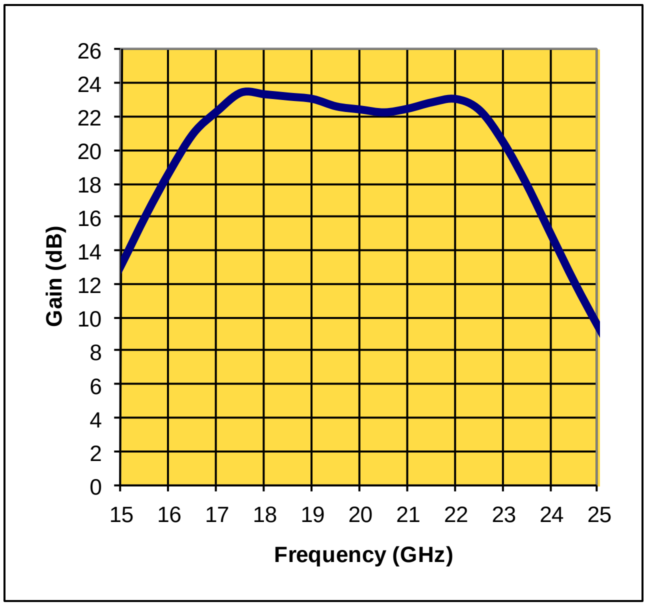

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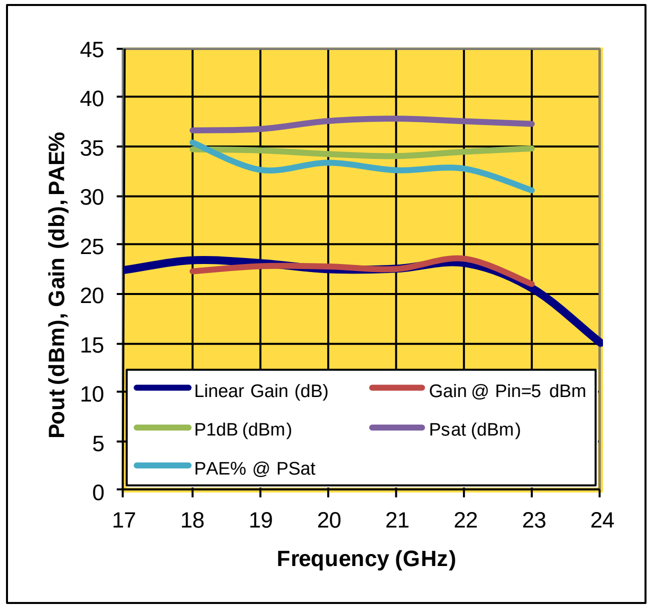

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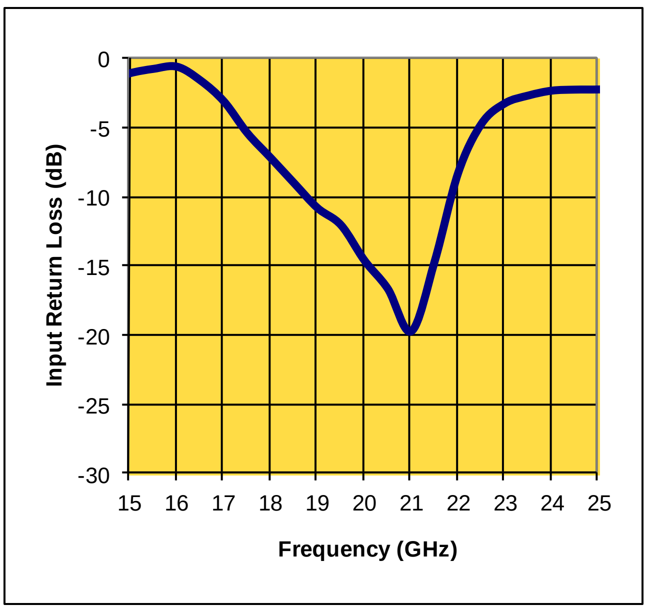

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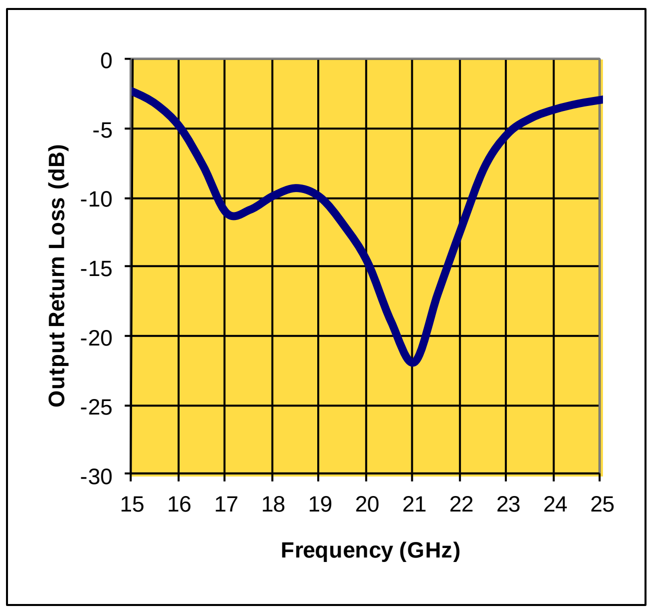

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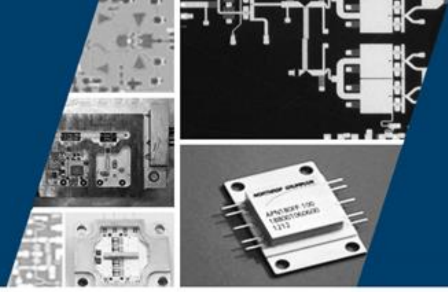

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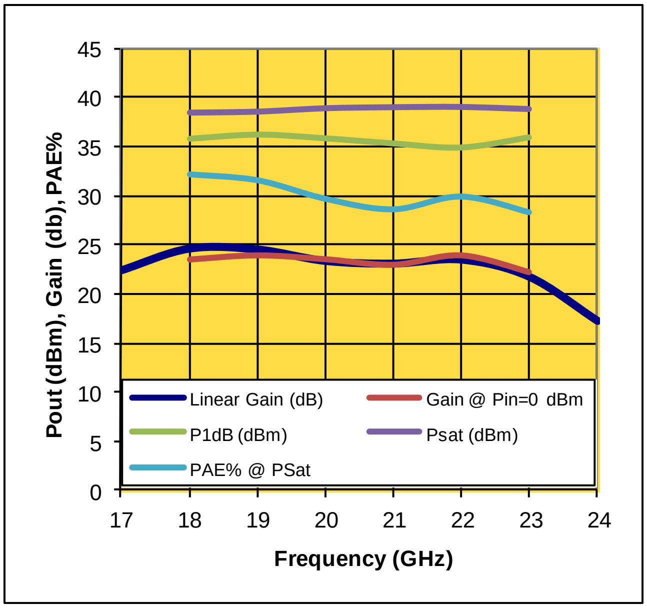
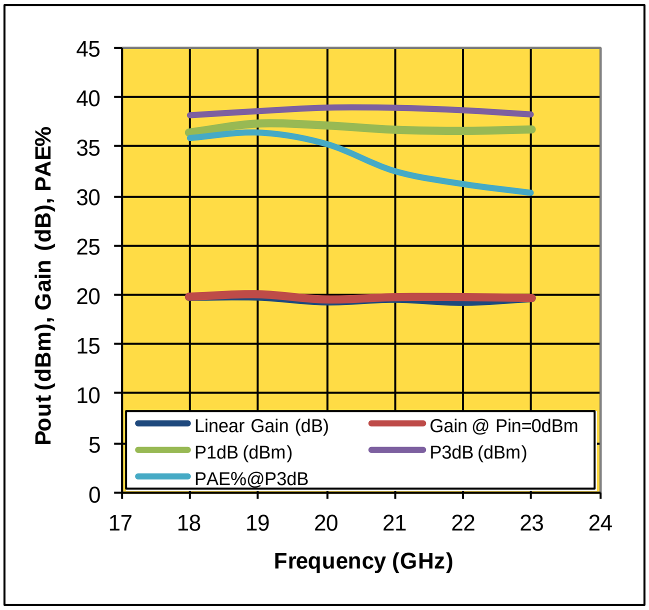
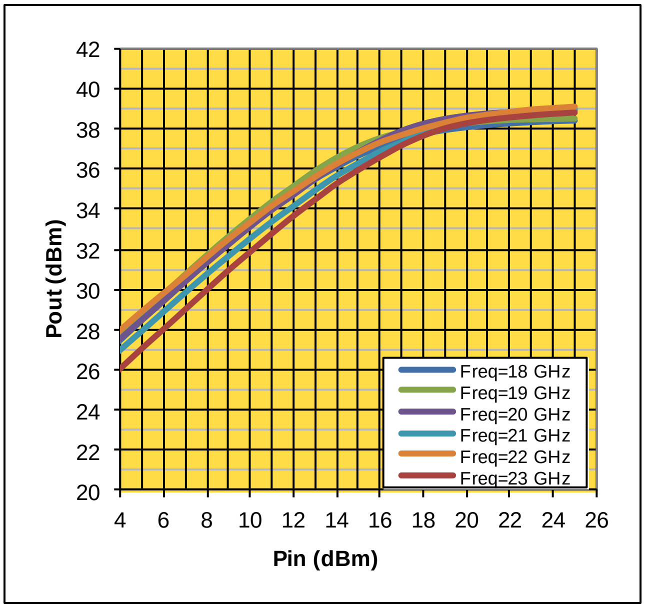


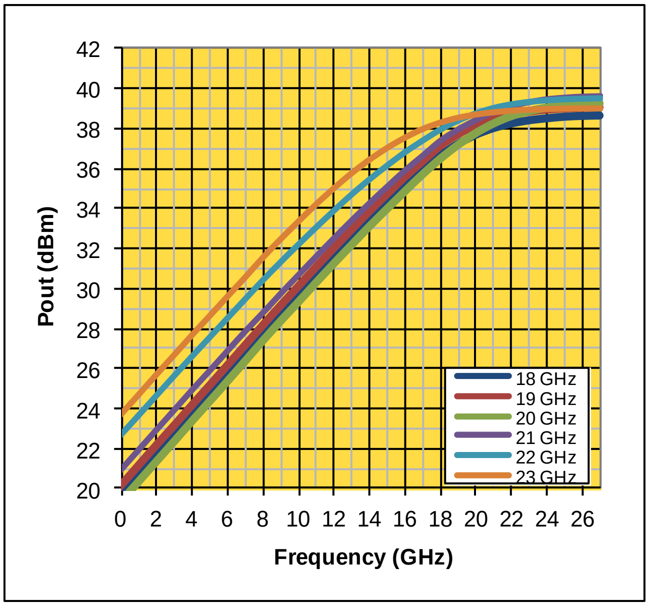
Power, Gain, PAE% vs. Frequency **



Output Power vs. Input Power *



Output Power vs. Input Power **



* Pulsed-Power On-Wafer, **CW in Fixture

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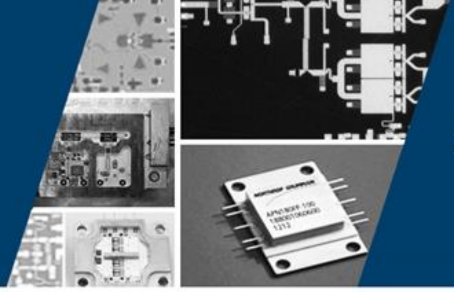

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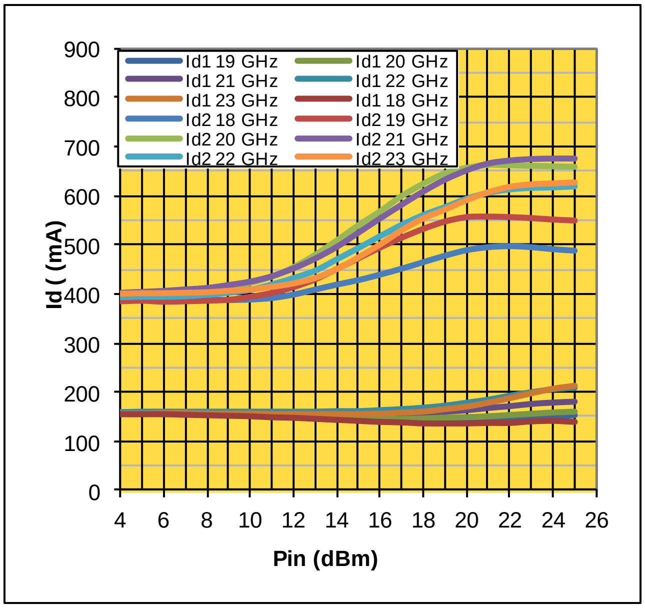
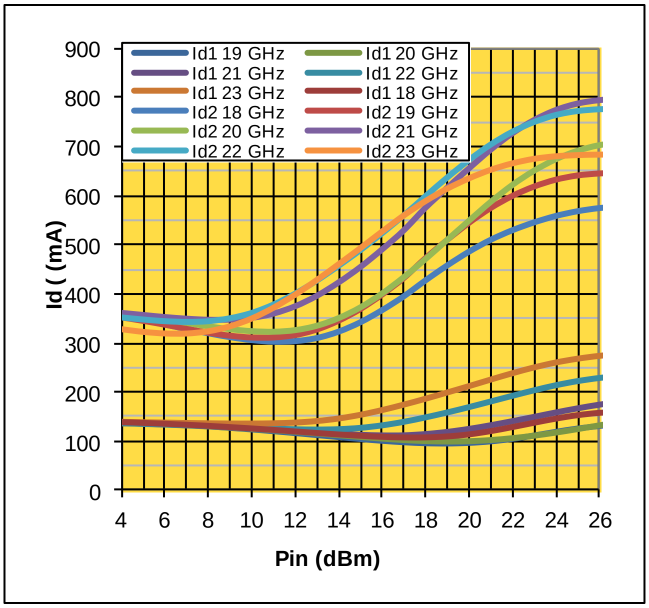
Power, Gain, PAE% vs. Frequency *



Power, Gain, PAE% vs. Frequency **



* Pulsed-Power On-Wafer, **CW in Fixture

Thermal Properties

Preliminary Thermal Properties with die mounted with 1mil 80/20 AuSn Eutectic to 25mil CuW Shim.

Conditions	Shim Boundary Temperature	Junction Temperature Tjc	Thermal Resistance θjc
Vd = 28V, Id1 = 140 mA * Id2 + Id2a = 727 mA * Pin=23.24 dBm Pout=39.14 dBm	25 ºC 50 ºC 57.3 ºC	152.2 ºC 189.1 ºC 200.0 ºC **	7.8 ºC/W 8.6 ºC/W 8.78 ºC/W

* Vd = 28.0 V, Idq1 = 144 mA, Id2q = 400 mA
** Max recommended. Pre-qualification reliability testing indicates that MTTF in excess of 10^5 hours can be achieved by ensuring Tjc is kept below 200ºC.

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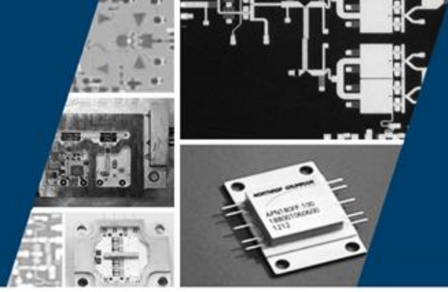

Measured Performance Characteristics (Typical Performance at 25°C)
Vd = 28.0 V, Id1 = 144 mA, Id2 = 400 mA *

Freq GHz	S11 Mag	S11 Ang	S21 Mag	S21 Ang	S12 Mag	S12 Ang	S22 Mag	S22 Ang
12.0	0.699	43.964	0.779	-19.442	0.002	36.788	0.840	-130.950
12.5	0.692	27.965	1.003	-37.868	0.001	-113.227	0.863	-143.724
13.0	0.702	13.013	1.304	-56.793	0.003	115.571	0.867	-157.606
13.5	0.701	-6.259	1.756	-75.707	0.003	12.387	0.861	-170.158
14.0	0.743	-23.885	2.312	-97.113	0.002	116.066	0.854	176.435
14.5	0.753	-41.896	3.187	-118.651	0.003	53.407	0.822	163.141
15.0	0.809	-61.628	4.308	-141.688	0.004	79.825	0.789	149.562
15.5	0.843	-81.659	5.968	-168.862	0.006	45.166	0.716	133.098
16.0	0.886	-106.151	8.076	160.835	0.006	19.273	0.597	116.578
16.5	0.893	-125.821	10.849	129.080	0.009	-0.556	0.443	99.724
17.0	0.830	-154.023	13.070	90.315	0.010	-38.819	0.255	87.416
17.5	0.713	-169.316	15.259	52.758	0.011	-68.439	0.152	126.751
18.0	0.558	168.254	15.601	13.681	0.010	-102.665	0.242	138.228
18.5	0.460	164.497	15.149	-18.903	0.011	-131.466	0.284	127.812
19.0	0.338	151.417	15.094	-50.296	0.012	-168.802	0.274	112.392
19.5	0.304	151.107	14.549	-80.833	0.012	159.721	0.231	91.740
20.0	0.215	144.657	14.221	-108.869	0.014	128.038	0.164	82.177
20.5	0.206	125.765	13.863	-138.643	0.011	101.178	0.109	65.615
21.0	0.089	135.731	14.090	-166.063	0.013	87.099	0.090	93.235
21.5	0.091	41.988	14.418	163.337	0.018	51.402	0.135	93.307
22.0	0.190	-58.964	14.261	126.963	0.017	16.108	0.220	56.643
22.5	0.439	-77.160	13.245	89.725	0.015	-15.227	0.324	10.566
23.0	0.560	-109.180	10.993	51.085	0.013	-49.790	0.447	-28.152
23.5	0.724	-128.470	8.148	18.278	0.009	-71.583	0.541	-61.608
24.0	0.727	-148.562	5.919	-11.422	0.007	-100.505	0.595	-85.387
24.5	0.802	-160.957	4.218	-34.985	0.003	-131.781	0.629	-104.385
25.0	0.777	-170.382	3.155	-57.268	0.002	-89.706	0.661	-119.136
25.5	0.803	177.352	2.293	-77.195	0.002	-49.011	0.681	-130.378
26.0	0.789	172.098	1.807	-94.490	0.001	-29.848	0.713	-139.718
26.5	0.775	157.890	1.382	-113.016	0.004	-0.197	0.733	-148.879
27.0	0.811	158.238	1.094	-127.212	0.004	-55.666	0.747	-156.758
27.5	0.767	147.132	0.861	-144.501	0.005	-81.846	0.757	-163.728
28.0	0.830	142.237	0.689	-158.251	0.001	-63.247	0.785	-170.694

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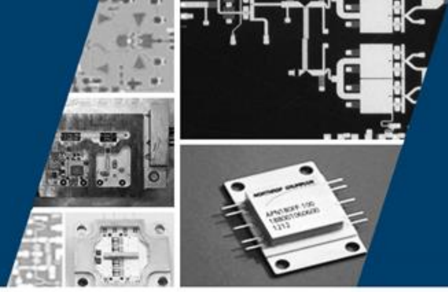
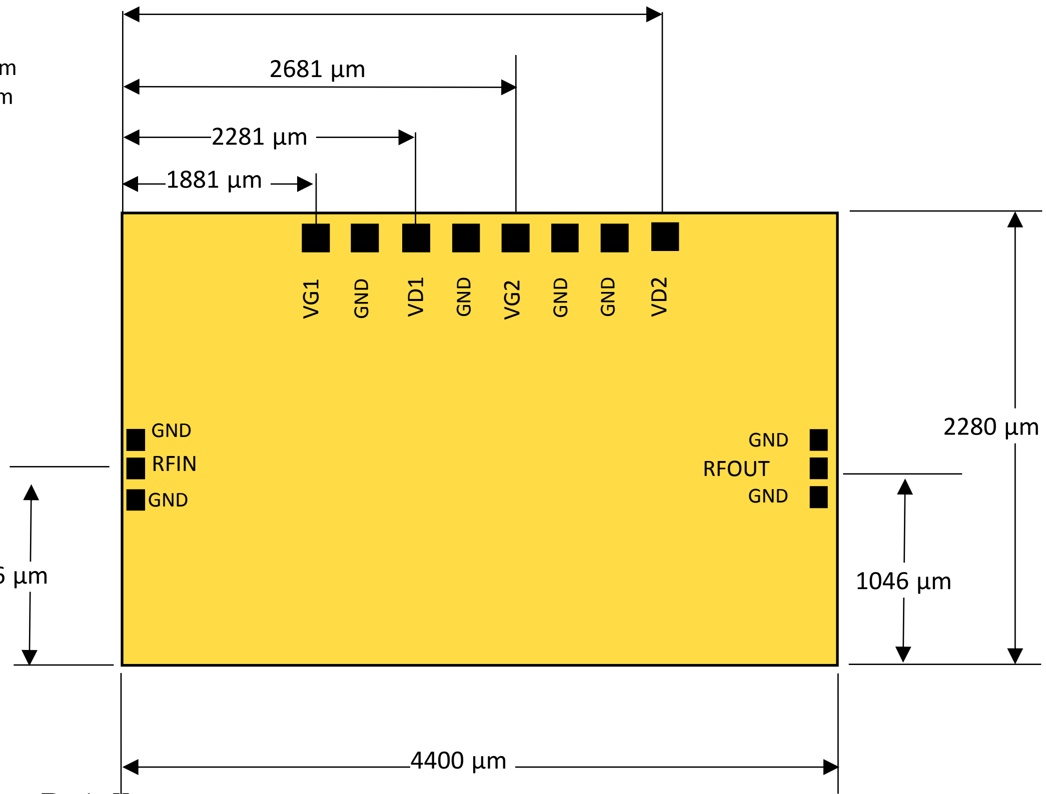


Die Size and Bond Pad Locations (Not to Scale)

X = 4400 µm ± 25 µm
Y = 2280 ± 25 µm
DC Bond Pad = 100 x 100 ± 0.5 µm
RF Bond Pad = 100 x 100 ± 0.5 µm
Chip Thickness = 101 ± 5 µm



Biasing/De-Biasing Details:
Bias is single sided and is from the top only.

Listed below are some guidelines for GaN device testing and wire bonding:

a. Limit positive gate bias (G-S or G-D) to < 1V
b. Know your devices' breakdown voltages
c. Use a power supply with both voltage and current limit.
d. With the power supply off and the voltage and current levels at minimum, attach the ground lead to your test fixture.
    i. Apply negative gate voltage (-5 V) to ensure that all devices are off
    ii. Ramp up drain bias to ~10 V
    iii. Gradually increase gate bias voltage while monitoring drain current until 20% of the operating current is achieved
    iv. Ramp up drain to operating bias
    v. Gradually increase gate bias voltage while monitoring drain current until the operating current is achieved
e. To safely de-bias GaN devices, start by debiasing output amplifier stages first (if applicable):
    i. Gradually decrease drain bias to 0 V.
    ii. Gradually decrease gate bias to 0 V.
    iii. Turn off supply voltages
f. Repeat de-bias procedure for each amplifier stage

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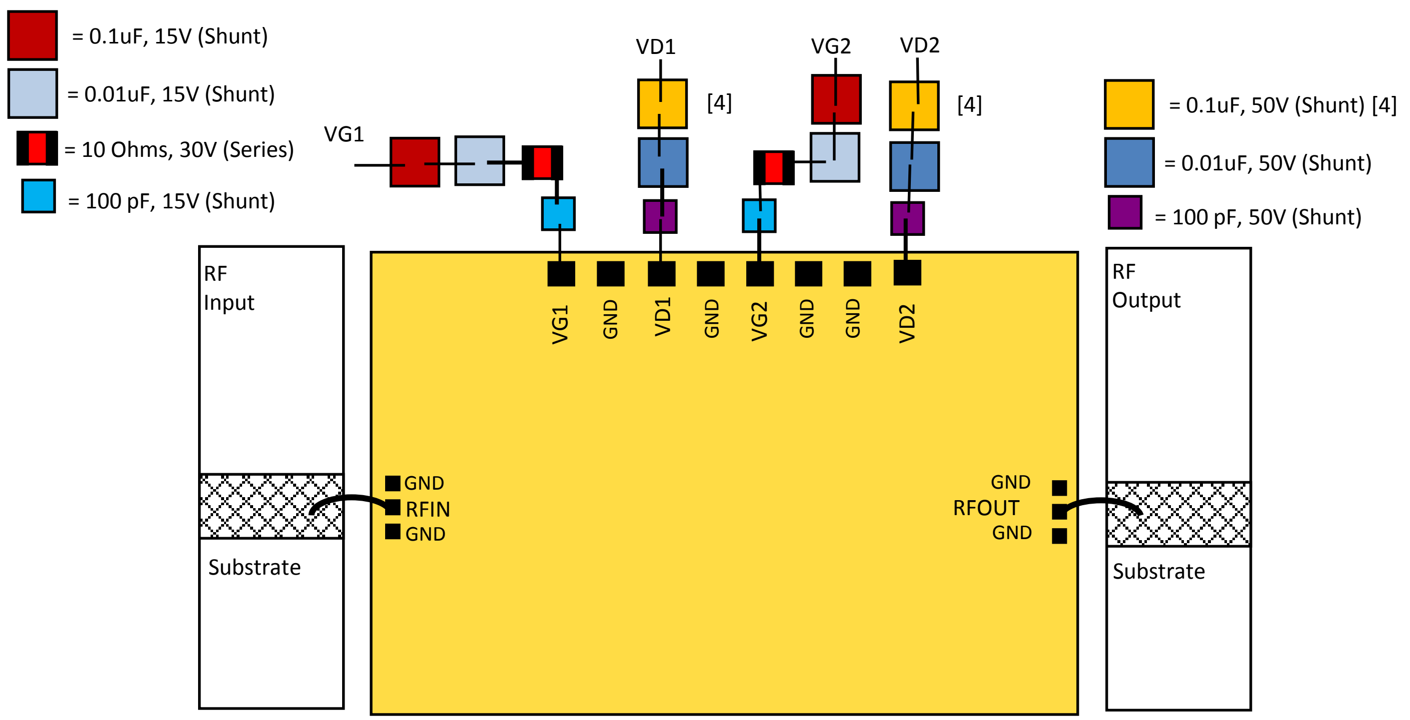
Suggested Bonding Arrangement



Recommended Assembly Notes

1. Bypass caps should be 100 pF (approximately) ceramic (single-layer) placed no farther than 30 mils from the amplifier.
2. Best performance obtained from use of <10 mil (long) by 3 by 0.5 mil ribbons on input and output.
3. Part must be biased from both sides as indicated.
4. The 0.1uF, 50V capacitors are not needed if the drain supply line is clean. If Drain Pulsing of the device is to be used, do **NOT** use the 0.1uF , 50V Capacitors.

Mounting Processes

Most NGAS GaN IC chips have a gold backing and can be mounted successfully using either a conductive epoxy or AuSn attachment. NGAS recommends the use of AuSn for high power devices to provide a good thermal path and a good RF path to ground. Maximum recommended temp during die attach is 320ºC for 30 seconds.

Note: Many of the NGAS parts do incorporate airbridges, so caution should be used when determining the pick up tool.

CAUTION: THE IMPROPER USE OF AuSn ATTACHMENT CAN CATASTROPHICALLY DAMAGE GaN CHIPS.

PLEASE ALSO REFER TO OUR "GaN Chip Handling Application Note" BEFORE HANDLING, ASSEMBLING OR BIASING THESE MMICS!

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