AQLVR02

RAD-HARD Quad 500 Mbps Bus LVDS Receiver

FEATURES

- 500.0 Mbps low jitter data path
- 3.3 V power supply
- CMOS/TTL compatible Inputs/Outputs
- Cold sparing on all pins
- 4ns Propagation delay in temperature range
- Very low skew
- Extended LVDS input common mode [-4V; +5] V
- Receiver input threshold ≤ ±100 mV
- 50 mV (min) Input hysteresis
- Fail Safe protection circuit
- Radiation tolerant: 300 krad(Si)
- Latch-up free up to 60 MeVcm^2/mg
- ESD tolerance: 8 kV
- 16-pins, Ceramic Flat Pack (FP-16).
- ANSI TIA/EIA 644a LVDS standard Compliant
- Space Quality level
- Optimum BER in radiation environment at maximum bit rate.

DESCRIPTION

ARQUIMEA's AQLVR02 device is a Quad Bus Low Voltage Differential Signals (LVDS) Receiver intended for low power, low noise and high-speed operation. The IC is optimized for operation above 500Mbps.

Data path consists in a fully differential LVDS input with its associated LVCMOS/LVTTL output.

The AQLVR02 allows high-speed LVDS data transmission for point-to-point or multi-drop interconnects. The device is specifically designed for the bridging of multiple backplanes in a system.

The Quad LVDS Receiver supports an overall TRI-STATE function that may be used to disable the output stages, disabling the load current, and thus dropping the device to an ultra-low idle power state.

All pins, including CMOS Input/outputs, have Cold Spare buffers. The pins will be high impedance when VDD is tied to VSS.

The input buffers of LVDS receiver include an active internal fail-safe circuit that sets the output of the receiver to a known high state when one or the two inputs floating, or inputs shorted.

The extended common mode range allows high voltage drops between ground planes without affecting performance.

APPLICATIONS

The AQLVR02 provides the basic bus receiver functions which allow isolation of segments or long-distance applications.

The intended application of these devices and signaling technique is for both space-wire point-to-point baseband (single termination) and multipoint (double termination) data transmissions over controlled impedance media.

The transmission media may be printed-circuit board traces, backplanes, or cables.

RADIATION HARDENING

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
TID	300	-	-	krad	1
SEL	60	-	-	MeV·cm^2/mg	
BER (tested at max Data Rate) for a GEO orbit	-	-	10^{-13}	Err/Bit/Day	

More information about radiation hardening features and radiation test conditions is available under request.

AVAILABLE OPTIONS

PRODUCT ORDERING Nº	QUALITY LEVEL	PACKAGE (*1)	OPERATING TEMPERATURE	VARIANT DETAIL	TERMINAL MATERIAL AND FINISH (*2)	DELIVERY PACK
AQLVR02E2	Engineering Model (*3)	16-pin Ceramic FP	-55ºC to 125ºC	NA	D2	15-pieces tray
AQLVR02S2	Space Flight Model (*4)	16-pin Ceramic FP	-55ºC to 125ºC	NA	D2	15-pieces tray

(*1) Other packaging options, including raw die format, are also available under request.
(*2) The terminal material and/or finish shall be in accordance with the requirements of ESCC23500
(*3) Only electrically tested at 25ºC
(*4) Space level screening and qualification per ESCC9000

Index

Glossary

BER	*Bit Error Ratio*
CMOS	*Complementary MOS FET*
ESD	*Electrostatic Discharge*
GEO	*Geostationary Earth Orbit*
IC	*Integrated Circuit*
LVCMOS	
LVDS	*Low Voltage Differential Signaling*
LVTTL	*Low Voltage Transistor-Transistor Logic*
PSRR	*Power Supply Rejection Ratio*
RL	*Load Resistor*
SEE	*Single Event Effect*
SEL	*Single Event Latch-up*
TID	*Total Ionizing Dose*
tf	*Fall Time*
tr	*Rise Time*
TTL	*Transistor-Transistor Logic*
VCM	*Common-mode voltage*
VID	*Differential Input Voltage*
VT	*Differential output voltage*
VTH	*Voltage High threshold*
VTL	*Low Voltage Threshold*

OVERVIEW

The AQLVR02 provides the basic bus receiver function. The device operates as a Quad LVDS Receiver. Receiving the LVDS amplitude and generating a LVCMOS/LVTTL digital output, allowing isolation of segments or long-distance applications.
The intended application of these devices and signaling technique is for both point-to-point baseband (single termination) and multipoint (double termination) data transmissions over controlled impedance media.

BLOCK DIAGRAM

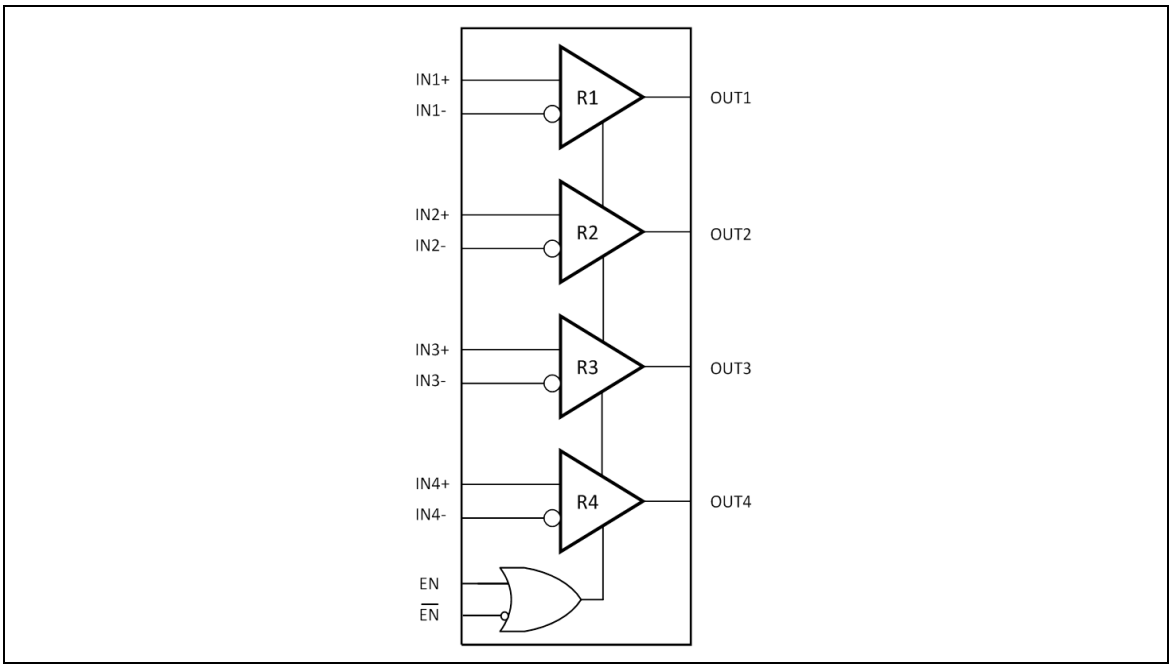


Figure 1: Block diagram

TRUTH TABLE

MODE	ENABLES		INPUTS	OUTPUTS
	EN	EN/	$V_{ID} = V_{IN+} - V_{IN-}$	OUT
Disabled	L or OPEN	H	X	Z
Enabled	H	X	$V_{ID} > V_{TH}$	H
	X	L or OPEN		
	H	X	$V_{TL} < V_{ID} < V_{TH}$	?
	X	L or OPEN		
	H	X	$V_{ID} < V_{TL}$	L
	X	L or OPEN		
Fail-Safe	H	X	OPEN/SC/Terminated for tFS>500ns	H
	X	L or OPEN		H

Table 1: Truth table

Notes:
(*) L= low Logic Level, H= High Logic Level, X= Irrelevant (L, OPEN or H), Z= High Impedance, '?'=Indeterminate

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	VALUE
V_{DD}	DC supply voltage	-0.5 V to 4.6 V
V_I	TTL/CMOS Input Voltage	-0.5 V to 6 V
V_{IN}	LVDS Input Voltage	-5 V to 6 V
T_{STG}	Storage temperature	-65°C to +150°C
T_J	Maximum junction temperature	+175°C
Tc	Maximum Case temperature	+125°C
ESD	ESD Last Passing Voltage – HBM	8 kV
P_D	Power dissipation	850mW

Table 2: Absolute Maximum Rating

Note: Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.

RECOMMENDED OPERATING CONDITIONS

The Recommended Operating as well as derated Conditions according to ECSS-Q-30-11A are presented below

SYMBOL	PARAMETER	OPERATING VALUES	DERATED VALUES
V_{DD}	Power supply voltage	3.0 V to 3.6 V	3.0 V to 3.6 V
V_{IN}	TTL/CMOS Input Voltage	0 V to 5 V	0 V to 5 V
	LVDS input voltage, receiver inputs	-4.6 V to 5.6 V	-4.6 V to 5.6 V
V_{CM}	LVDS Input Common Mode Voltage	-4 V to 5 V	-4 V to 5 V
T_C	Case temperature range	-55°C to +125°C	+100ºC (Tj=110ºC)

Table 3: Recommended Operating Conditions

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for V_{DD} = 3.3 V ± 0.3 V, -55°C < TC < +125°C

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
TTL/CMOS INPUT DC SPECIFICATIONS (EN, ENn)					
V_{IH}	High-level input voltage		2.0	5V	V
V_{IL}	Low-level input voltage		-0.3	0.8	V
I_{IH}	High-level input current	V_{DD} = 3.6V, V_{IN} = 3.6V;	-10	+10	µA
I_{IL}	Low-level input current	V_{DD} = 3.6V, V_{IN} = 0V	-10	+10	µA
I_{CS}	Cold Spare Leakage current	V_{DD} = V_{SS}, V_{IN} = 3.6V	-5	+5	µA
TTL/CMOS OUTPUT DC SPECIFICATIONS (OUT)					
V_{OH}	High-level output voltage	V_{DD} = 3.0V	2.4	V_{DD}	V
		V_{DD} = 3.0V, I_{OH} = -0.4mA	2.2	V_{DD}	V
		V_{DD} = 3.0V, I_{OH} = -2mA	2.2	V_{DD}	V
V_{OL}	Low-level output voltage	V_{DD} = 3.0V, I_{OL} = 2mA	-0.3	0.4	V
I_{CS}	Cold Spare Leakage current	V_{DD} = V_{SS}, V_{OUT} = 3.6 V	-15	+15	µA
I_{OZ}	Output Tri-State Current	V_{DD} = 3.6V, Tri-State output (channel disabled), V_{OUT} = V_{DD} or V_{SS}	-15	+15	µA
I_{OS}	Output Short Circuit Current (Only one output should be shorted at a time during short time)	V_{DD} = 3.6V, High Level output, V_{OUT} = 0 V		-150	mA
LVDS RECEIVER DC SPECIFICATIONS (IN+, IN-)					
V_{TH}	Differential Input High Threshold	V_{CM} = -4V to +5V		+100	mV
V_{TL}	Differential Input Low Threshold	V_{CM} = -4V to +5V	-100		mV
V_{ID_HYS}	Differential Input hysteresis	V_{TH} - V_{TL}	50		mV
V_{FSH}	Differential Input Fail-Safe High Threshold	V_{CMI} = -4V, +1.2V, +5V, Hold time>500ns	+10		mV
V_{FSL}	Differential Input Fail-Safe Low Threshold	V_{CMI} = -4V, +1.2V, +5V, Hold time>500ns		-10	mV
V_{CMR}	Common Mode Voltage Range	V_{ID}=±200mV (400mVpp)	-4	+5	V
I_{IN}	LVDS Input Current	V_{DD} = +3.6V, V_{CMI} = +1.2V, V_{ID}=±400mV	-10	+10	µA
		V_{DD} = +3.6V, V_{CMI} = -4V to +5V, V_{IN+}=V_{IN-}=V_{CMI}	-40	+40	µA
ΔI_{IN}	Input Current Balance (I_{IN+}-I_{IN-})	V_{DD} = +3.6V, V_{CMI} = -4V to +5V, V_{IN+}=V_{IN-}=V_{CMI}	-6	+6	µA
I_{CSIN}	Cold Sparing Leakage Current	V_{DD} = V_{SS}, V_{CMI} = +1.2V, V_{ID}=±400mV	-10	+10	µA
		V_{DD} = V_{SS}, V_{CMI} = -4V to +5V, V_{IN+}=V_{IN-}=V_{CMI}	-40	+40	µA
C_{IN}	Input Capacitance			3	pF
SUPPLY CURRENT					
I_{CLLS}	Total Supply Current	ENn = V_{SS}, EN = V_{DD}, V_{DD} = 3.6 V, Fq = DC, no load		60 (45 typ)	mA
I_{CCZ}	Tri-State Supply Current	ENn = V_{DD}, EN = V_{SS}, V_{DD} = 3.6 V, no load		10 (6 typ)	mA

Table 4: DC Electrical Characteristics

AC SWITCHING CHARACTERISTICS

Unless otherwise stated, these specifications apply for VDD = 3.3 V ± 0.3 V, TA = -55°C to +125°C.

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
t_{PHZ}	Disable Time (Active to Tri-State) High to Z	C_L = 10 pf (see Figure 5)		10	ns
t_{PLZ}	Disable Time (Active to Tri-State) Low to Z	C_L = 10 pf (see Figure 5)		10	ns
t_{PZH}	Enable Time (Tri-State to Active) Z to High	C_L = 10 pf (see Figure 5)		150	ns
t_{PZL}	Enable Time (Tri-State to Active) Z to Low	C_L = 10 pf (see Figure 5)		150	ns
t_{LHT}	Rise Time, 20% to 80%	C_L = 10pf		1.2	ns
t_{HLT}	Fall Time, 80% to 20%	C_L = 10pf		1.2	ns
t_{PLHD}	Propagation Low to High Delay	C_L = 10 pf		4.5	ns
T_{PHLD}	Propagation High to Low Delay	C_L = 10 pf		4.5	ns
T_{SKEW}	Differential Skew T_{PHLD} - T_{PLHD}			300	ps
T_{CCS}	Output Channel-to-Channel Skew			500	ps
T_{DDS}	Output Device-to-Device Skew			750	ps
t_{PJ}	Periodic Jitter	V_{ID}=±200mV (400mVpp), 50% duty cycle at 250MHz, trise≤ 1ns (20% - 80%)		15	ps
t_{CCJ}	Cycle to Cycle Jitter	V_{ID}=±200mV (400mVpp), 50% duty cycle at 250MHz, trise≤ 1ns (20% - 80%)		40	ps
t_{PPJ}	Peak to Peak Jitter	V_{ID} = $2^{\wedge(7)}$-1 PRBS pattern at 500Mbps, trise ≤ 1ns (20% - 80%)		250	ps
t_{DJ}	Deterministic Jitter	V_{ID} = $2^{\wedge(7)}$-1 PRBS pattern at 500Mbps, trise ≤ 1ns (20% - 80%)		200	ps

Table 5: AC Electrical Characteristics

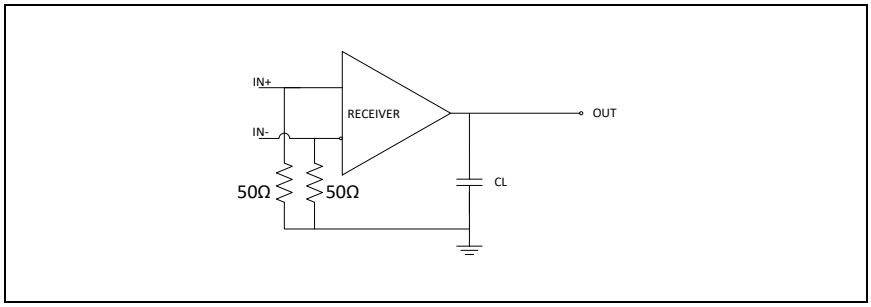


Figure 2: LVDS Test circuit Input/Output load

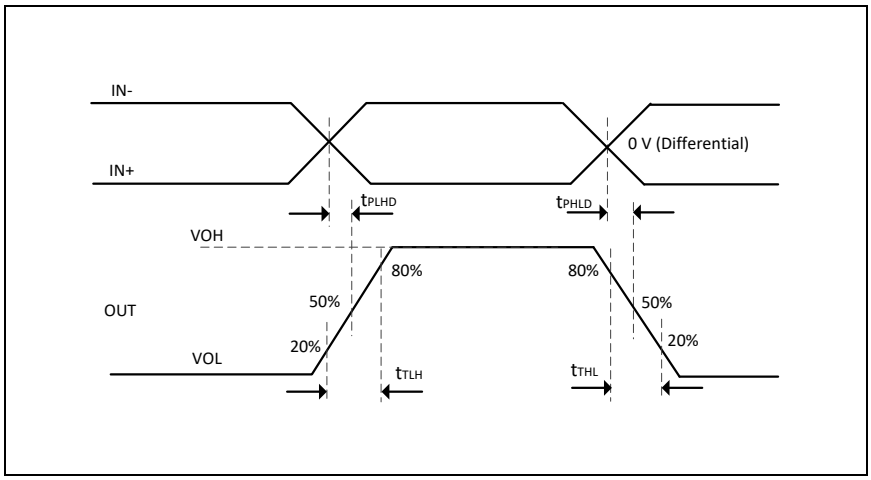


Figure 3: LVDS Propagation delay and transition time

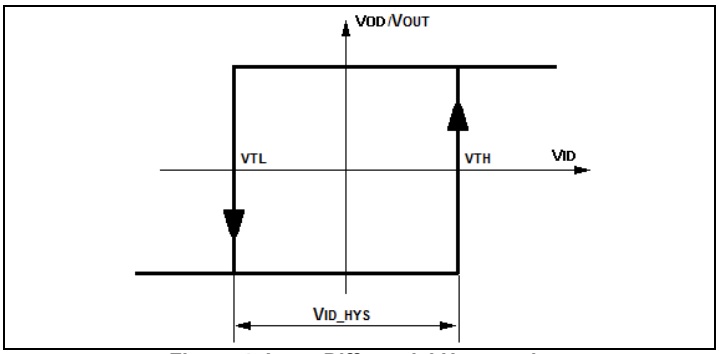
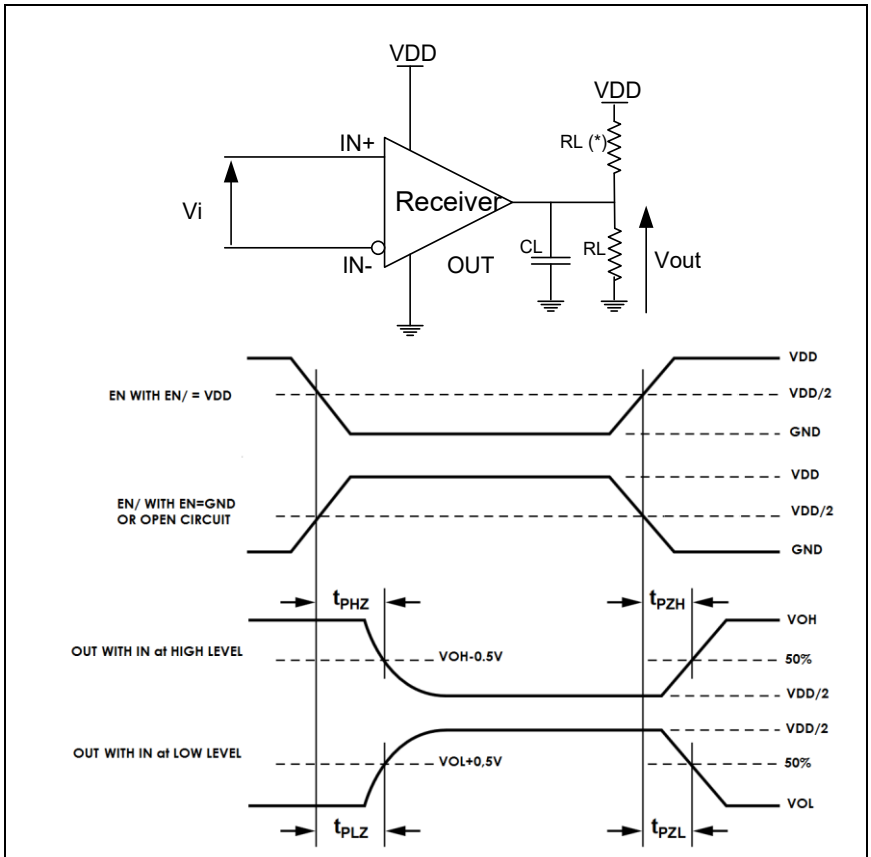


Figure 4: Input Differential Hysteresis



(*)Notes: RL=400 Ohm, Pull-up for t_{PLZ} and t_{PZL}; Pull-down for t_{PHZ} and t_{PZH}; CL=10pF;
Enable pulses are supplied by a generator with the following characteristics: tr or tf ≤ 1 ns, f = 500 kHz, and pulse width = 500 ns.

Figure 5: Output active to TRISTATE and TRISTATE to active

APPLICATIONS INFORMATION

Transmission media:

The transmission media may be printed-circuit board traces, backplanes, or cables. (Note: The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other application specific characteristics.)
The signal path should be matched in length to avoid any skew in differential lines or between channels.

Input Fail-Safe (comparator and timer)**:**
The AQLVR02 also supports Fail-Safe operation when OPEN or SHORTED inputs are present. Receiver output goes HIGH after 500 ns for all fail-safe conditions.

PCB layout and Power System Bypass:

Circuit board layout and stack-up for the AQLVR02 should be designed to provide noise-free power to the device.
Good layout practice also will separate high frequency or high-level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (4 to 10 mils) for power/ground sandwiches. This increases the intrinsic capacitance of the PCB power system which improves power supply filtering, especially at high frequencies, and makes the value and placement of external bypass capacitors less critical. A 0.25 Ω resistor is recommended in the power supply line path. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use value of 0.1 µF. Tantalum capacitors may be 2.2 µF. Voltage rating for tantalum capacitors should be at least 5x the power supply voltage being used. It is recommended practice to use two vias at each power pin of the AQLVR02, as well as all RF bypass capacitor terminals. Dual vias reduce the interconnect inductance and extends the effective frequency range of the bypass components.
The outer layers of the PCB may be flooded with additional ground plane. These planes will improve shielding and isolation, as well as increase the intrinsic capacitance of the power supply plane system. Naturally, to be effective, these planes must be tied to the ground supply plane at frequent intervals with vias. Frequent via placement also improves signal integrity in signal transmission lines by providing short paths for image currents which reduces signal distortion. The planes should be pulled back from all transmission lines and component mounting pads a distance equal to the width of the widest transmission line from the internal power or ground plane(s) whichever is greater. Doing so minimizes effects on transmission line impedances and reduces unwanted parasitic capacitances at component mounting pads.
It is recommended to adapt CMOS outputs to the transmission lines characteristic impedance with a serial resistance to improve signal integrity.
The serial resistance must verify the equation:

$$Rs = Z_L - Z_O, \text{ where:}$$

Rs = Series resistance;
Z_L= transmission line characteristic impedance;
Z_O = CMOS output impedance.

The impedance of the CMOS outputs is not a controlled parameter and may present a small chip – to – chip variation, but its value is around 3 Ohms.

PINOUT DESCRIPTION

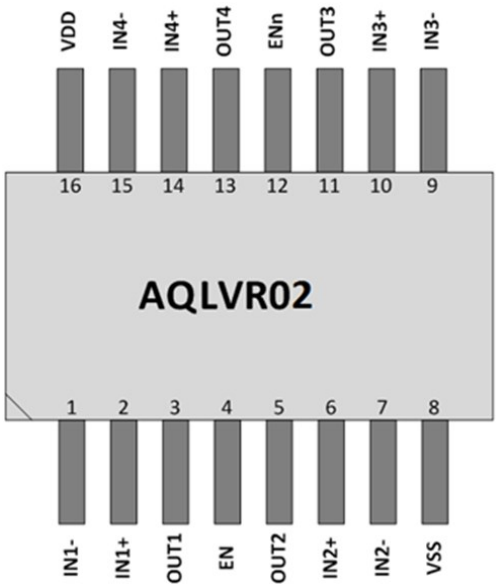


Figure 6: Pinout diagram

Pin Nº	Name	Type	Description
1	IN1-	LVDS Input	Inverting LVDS input, channel 1
2	IN1+	LVDS Input	Non-Inverting LVDS input, channel 1
3	OUT1	Digital Output	CMOS/TTL output, channel 1
4	EN	Digital Input	Logic enable for the LVDS receivers
5	OUT2	Digital Output	CMOS/TTL output, channel 2
6	IN2+	LVDS Input	Non-Inverting LVDS input, channel 2
7	IN2-	LVDS Input	Inverting LVDS input, channel 2
8	VSS	Power	Ground
9	IN3-	LVDS Input	Inverting LVDS input, channel 3
10	IN3+	LVDS Input	Non-Inverting LVDS input, channel 3
11	OUT3	Digital Output	CMOS/TTL output, channel 3
12	ENn	Digital Input	Logic active low enable for the LVDS receivers
13	OUT4	Digital Output	CMOS/TTL output, channel 4
14	IN4+	LVDS Input	Non-Inverting LVDS input, channel 4
15	IN4-	LVDS Input	Inverting LVDS input, channel 4
16	VDD	Power	3.3 V Power

Table 6: Pinout description

PACKAGE

FP16 Drawing

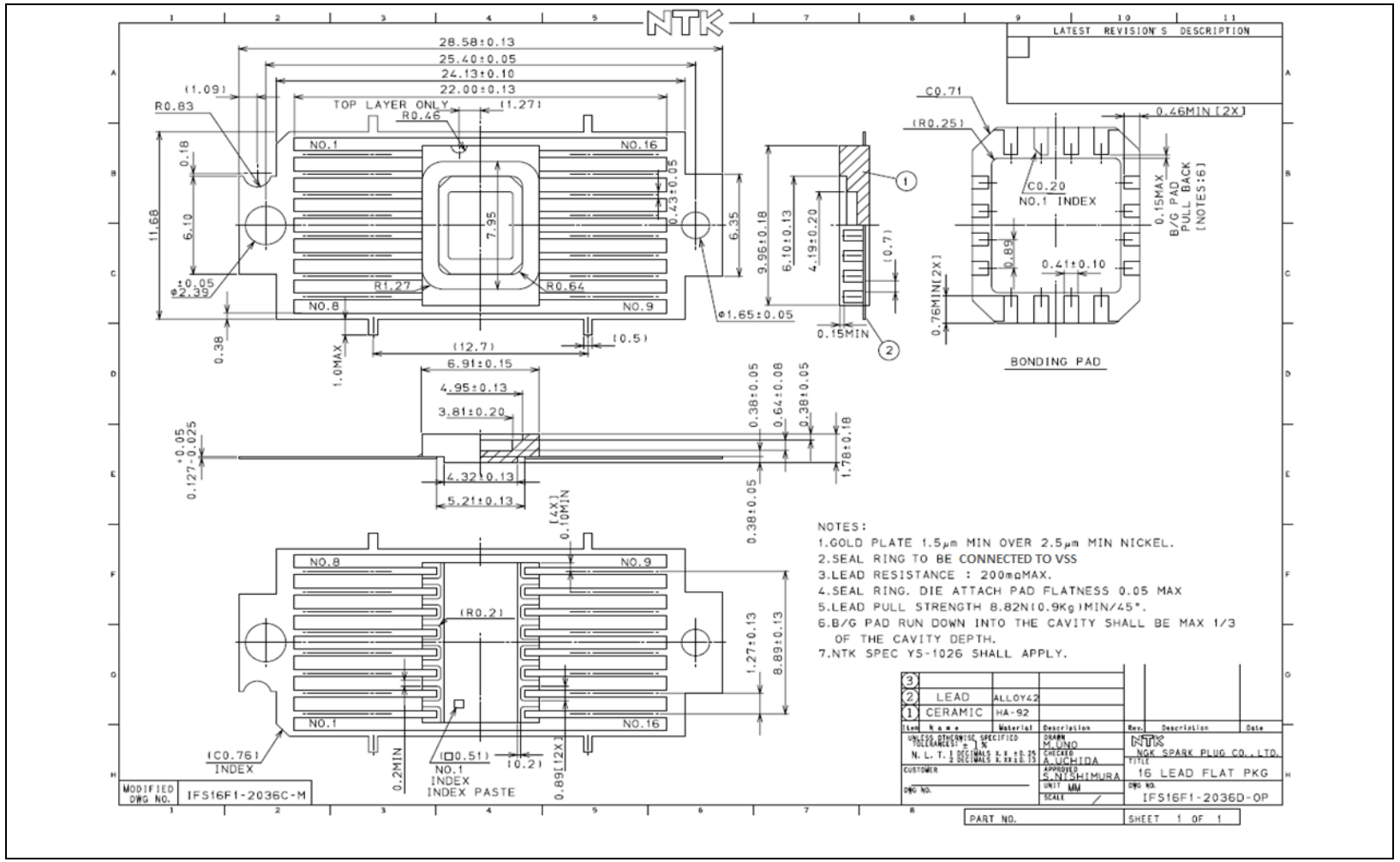


Figure 7: FP-16 Package drawing

Notes:
1. An Index mark shall be located adjacent to Pin 1.
2. The dimension shall be measured from the seating plane to the base plane.
3. The true position pin spacing is 1.27mm between centerlines. Each pin centerline shall be located within ±0.13mm of its true longitudinal position relative to Pin 1 and the highest pin number.
4. All exposed metalized areas are gold plated over electroplated nickel per MIL-PRF-38535.
5. The lid is electrically connected to VSS.
6. Lead finishes are in accordance to MIL-PRF-38535.

MARKING

The laser marked information on the component are:

- ARQUIMEA's symbol
- The Entire Part-type
- Traceability information

The traceability information comprises a manufacturing date code, a lot identification and a serial number:

- **Date Code**: Four-digit code number is used for the manufacturing date. The first two digits are the last two figures of the year of manufacture. The last two digits indicate the week of the year (i.e. 01 to 52), during which encapsulation or the final production process occurred.

- **Lot and Selected Sublot Identification**: If it is necessary to differentiate between more than one lot processed in the same week, a suffix letter (beginning with the letter A) is added to the date code. For a Selected Sublot a second suffix letter (beginning with the letter A) is added to the date code. For a single lot or sublot, letters are omitted (replaced by space).

- **Serial Number**: A serial number consisting of three digits is used. Serial numbers are run sequentially and not duplicated if more than one sub-lot is taken from one production lot.

QUALITY STANDARDS

ARQUIMEA ADS S.L.U. develops its activities under the premises of quality and sustainability, offering efficient, liable and innovative technologies and solutions to its customers.

ARQUIMEA's Quality Management System meets the requirements of UNE-EN 9100:2018 Aerospace Series and has been audited and certified by the Spanish Association for Standardization and Certification, AENOR.

To meet the highest quality and reliability, ARQUIMEA designs and develops its aerospace product line according to military and space standards.

Our space microelectronic devices are available in the following processes (Screened and Qualified):

- Equivalent to QML 38535 LEVEL Q or V* (on request)
- Equivalent to ESCC 9000*

*with radiation Qualification

For the procurement in die form, the following processes can be offered on request:

- In accordance with ECSS-Q-ST-60-05C
- Equivalent to QML 38534 LEVEL H or Level K*

Engineering Models are available and tested at 25ºC only.
*With Radiation Qualification

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REVISION HISTORY

Date Released	Issue	Section	Changes
12-05-2016	Draft A	All	Initial Release
23-09-2016	Draft B	ELECTRICAL CHARACTERISTICS	Parameter update after electrical Measurements
		AC SWITCHING CHARACTERISTICS	
20-09-2017	Draft C	ELECTRICAL CHARACTERISTICS	I_{CLLS} parameters added, Hysteresis feature and Failsafe Threshold Added
		AC SWITCHING CHARACTERISTICS	Jitter parameter added
30-10-2017	Issue 01	All	Minor Format Review
28-11-2017	Issue 02	TRUTH TABLE	Added table
20-02-2018	03	AVAILABLE OPTIONS PACKAGE MARKING	Added description Notes Added Added Information
01-07-2018 01-10-2018	04 05	ELECTRICAL CHARACTERISTICS	Parameter update after Electrical Measurements at room temperature
10-01-2019	06	ALL	Part-type AQLVR02 replaces ARQ-LVR002 Parameters limit update
02-09-2019	07	ELECTRICAL CHARACTERISTICS	Parameter update after Electrical Measurements at room temperature on AQLVR02S2
23-09-2019	08	ELECTRICAL CHARACTERISTICS	Parameter update after Electrical Measurements at room temperature on AQLVR02S2
06-11-2019	01	ALL GLOSSARY MARKING QUALITY STANDARDS	Datasheet code has been changed, 17501 instead of 15601 Non applicable terms have been deleted. ARQUIMEA logo has been updated. ISO 9100:2010 has been updated, UNE-EN 9100:2018 is the applicable now.
28-11-2019	02	Page 8	Added Pull-Up and Pull-Down description

ARQUIMEA

Space Technology Partner

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