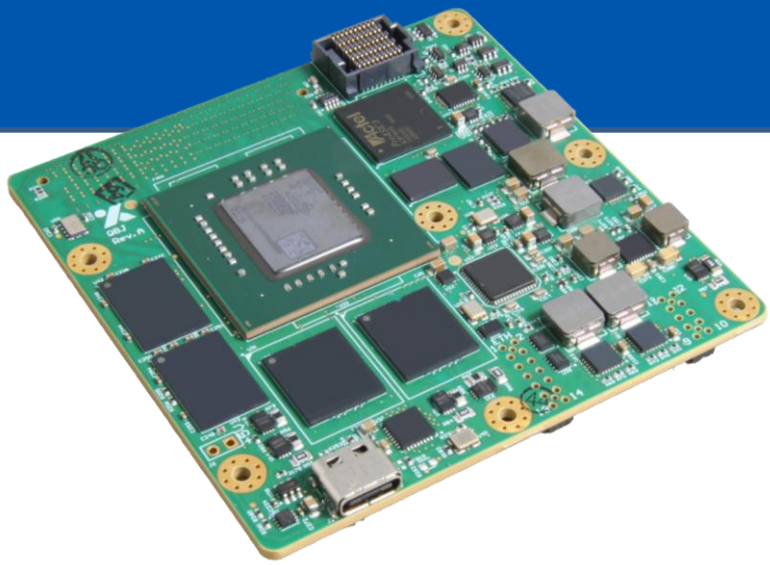
Q8J SPECIFICATIONS



Q8J

FEATURE HIGHLIGHTS

Industry-Leading Performance	The Q8J features a Multi-Processor System-on-Chip (MPSoC), including multi-core CPUs providing 64-bit processor scalability supported by massive programmable logic resources and a wide array of hardware interfaces.
Low Mass, Volume, Power	The Q8J measures 80 mm x 80 mm x 11.2 mm and consumes as little as 4 W. Its small size, low mass and power consumption make the Q8J ideal for aerospace applications that demand extremely high performance.
Integrated Hybrid Environment	The application space in a Q8J is a tight integration of a quad-core ARM Cortex-A53 Application Processing Unit, a dual-core ARM Cortex-R5 Real-Time Processing Unit, an ARM Mali-400 GPU and programmable logic, featuring 504,000 system logic cells, 461,000 flip-flops, 274,000 lookup tables and 1,728 DSP slices reserved for application-specific use.
Flexible Interfacing	The Q8J provides Gigabit Ethernet networking through its RJ45 connector (on adapter) along with USB 2.0 & USB 3.1 Gen 1 host ports. The Q8J also provides multiple digital I/O lines, including up to 68 SE GPIO, 12 MIO, 50 LVDS pairs, 17 Gigabit transceivers (full duplex) + 5 clock references, USB 2.0 and factory-selectable RS-232/422/485 through its mezzanine connector. The Gigabit transceivers can support JESD204B to interface with high speed ADCs, DACs and RF transceivers.
Applications	The extremely high performance and extensive FPGA fabric make the Q8J ideally suited for onboard: • Synthetic Aperture Radar (SAR) processing • Hyper/multispectral compression • Stereo and monocular visual odometry • Image registration and alignment • Convolutional neural networks • Advanced Software Defined Radios (SDR)

OVERVIEW

The Q8J extends the capability of the Xiphos Q8 processor, adding support for high speed JESD204B interfaces as well as access to external DDR3 or DDR4 memory. The Q8J is ideal for advanced SDR applications.

At the core of each Q8J is a hybrid environment of powerful multi-core CPUs, and reprogrammable logic, providing consistent and reliable performance. The library of logic and software functions is augmented by onboard digital I/O and high speed transceivers enabling JESD204B interfaces with high performance ADCs, DACs, and RF transceivers.

FLIGHT HERITAGE

The Q8J is the latest in the line of space qualified Q-Cards. The Q8J's predecessors include the Q8, Q7, Q6, Q5 and Q4:

- The Q8S was first flown in September 2020.
- The Q7S has been operating in orbit since June 2016. The Q7S is certified for manned space flight and is used on the International Space Station (ISS).
- The Q6S was first flown in August 2011, with almost 100 units delivered to customers worldwide. It was also certified for manned space flight and used on the ISS.
- The Q5S was first flown in June 2004.
- The Q4S was first flown in December 2002 and was also certified for manned space flight and used on the ISS.

Xiphos Technologies

Q8J

Front & Back

Product Integration Module (PIM)
Each Q8J is delivered with a detachable PIM to facilitate development. The PIM provides standard commercial interfaces (e.g. CAN, 1-wire, 4 RSXXX, JTAG, 13 digital I/O, 8 analog input, 4 analog output), debug LEDs and other lab development features.

Software Development
Xiphos provides an Application Development Kit with standard Linux libraries for C/C++ to support software development on Linux workstations. ***Code previously developed for Linux desktop and server applications can be easily ported to the Q8J.*** Q8J hardware and logic interfaces are all accessible through either standard Linux and Xilinx kernel drivers or custom drivers provided by Xiphos.

Logic Development
Logic development uses standard Xilinx development tools. Xiphos, Xilinx and many third-party vendors also provide a wide range of compatible reusable logic cores for Xilinx FPGAs.

Xiphos Technologies

Characteristics

(Rev B Board)

Memory
- 4 GB LPDDR4 DRAM
- 2x 256 MB QSPI Flash (NOR)
- External PL-accessible DDR3 or DDR4 DRAM
- 2x eMMC, 128 GB each, on independent buses / power control

Multi-Processor System-on-Chip
- Xilinx Zynq UltraScale+ XCZU7EG
- Quad-core ARM Cortex-A53 Application Processing Unit at up to 1.2 GHz
- Dual-core ARM Cortex-R5 Real-Time Processing Unit at up to 500 MHz
- ARM Mali-400 GPU at up to 600 MHz
- 504,000 system logic cells
- 461,000 flip-flops (FF)
- 274,000 lookup tables (LUT)
- 1,728 DSP slices

Control FPGA
- Microsemi ProASIC3

Operating System
- Linux 4.14 LTS
- Robot Operating System (ROS)

Real Time Clock
- RTC with sleep & wake-up on alarm/interrupt
- Dedicated power pin for external battery

Power
- 4 W - 25 W, scalable
- 6 to 16 VDC
- Various power modes (including deep sleep)
- Overcurrent detection & protection (global and local) and brownout protection

Form Factor
- 80 mm x 80 mm x 11.2 mm, 56 g (without connectors)

Environmental
- Operating Temperature -40 to +60ºC

Interfaces
- Power
- Gigabit Ethernet (RJ45 on adapter)
- USB 2.0 & USB 3.1 Gen 1 hosts (USB C)
- CAN Bus & PCIe controllers
- Up to 25 single-ended GPIO 3.3 V, 43 single-ended GPIO 1.8 V, 12 MIO 1.8 V, 50 LVDS pairs/100 single-ended GPIO 1.8 V, 16 PL GTH transceivers (up to 12.5 Gbps for JESD204B, PCIe) + 4 clock references, 1 PS GTR transceiver (up to 6 Gbps, for SATA, PCIe), USB 2.0 and factory-selectable RS-232/422/485 (Mezzanine connector)

Space-Qualified Features (Q8JS)
- Triple-mode redundancy (ProASIC3)
- EDAC-protected RAM
- Upset and multi-current monitoring
- Overcurrent protection (multiple)
- FPGA bit-stream scrubbing
- Software robustness / watchdog, etc.

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