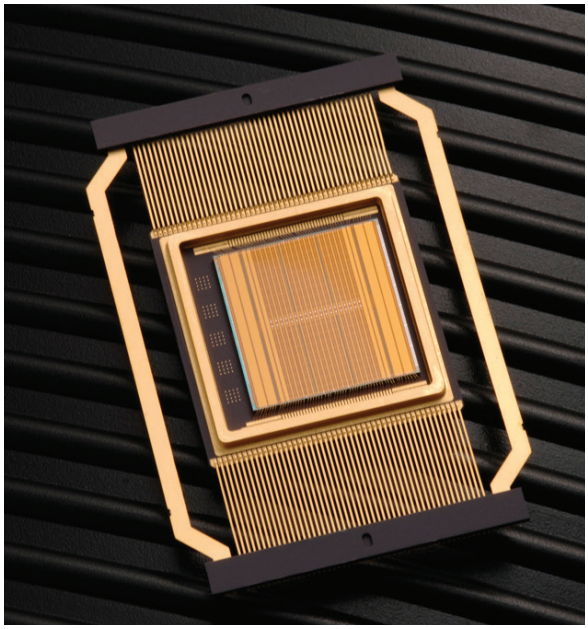
BAE SYSTEMS
INSPIRED WORK

Monolithic 16M radiation-hardened SRAM



High-speed memory product

The monolithic 16 Mb static random access memory is BAE Systems' next-generation, radiation-hardened memory product for users in the space community.

Description

Capable of withstanding the effects of natural space and an upper radiation-hardened environment, the 16 Mb monolithic SRAM has total-dose tolerance of greater than 1 Mrad and an upset rate of less than 1E-12 upsets per bit-day. Prompt dose levels are >1E9 rad/sec.

Key features

- Read and write access time 13.5 ns typical, 17 ns and 20 ns worst case
- Operating temperature range -55 degrees Celsius to +125 degrees Celsius
- Operating voltage (core) 1.5V
- Operating voltage (I/O) 3.3V
- Standby power < 2 mW typical, < 100 mW worst case
- Operating power < 7.5 mW/MHz typical
- Packaging 86-lead ceramic flatpack
- Asynchronous operation
- Prototype and flight flows
- Latchup-immune

System definitions

A:0-20 Address input pins that select a particular 8-bit word within the memory array.

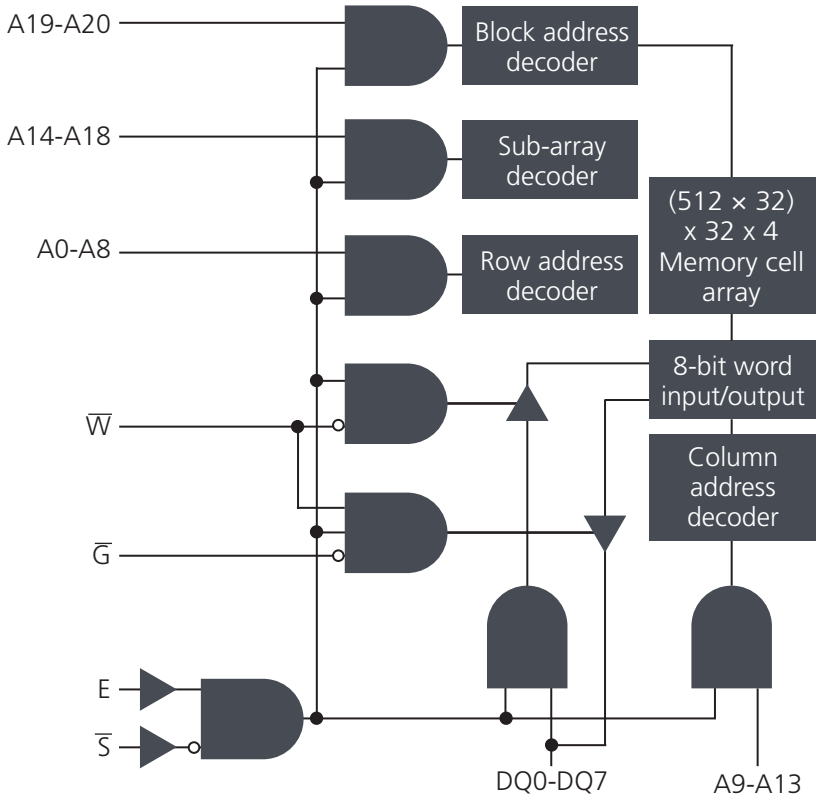
DQ:0-7 Bi-directional data pins that serve as data outputs during a read operation and as data inputs during a write operation.

$\overline{S}$ Negative chip select at a low level allows normal read or write operation. At a high level, $\overline{S}$ forces the SRAM to a precharge condition, holds the data output drivers in a high-impedance state, and disables only the data input buffers. If this signal is not used, it must be connected to GND.

$\overline{W}$ Negative write enable at a low level activates a write operation and holds the data output drivers in a high-impedance state. At a high-level $\overline{W}$ allows normal read operation.

$\overline{G}$ Negative output enable at a high level holds the data output drivers in a high-impedance state. At a low level, the data output driver state is defined by $\overline{S}$, $\overline{W}$, and E. If this signal is not used, it must be connected to GND.

E Chip enable at a high level allows normal operation. At a low level, E forces the SRAM to a precharge condition, holds the data output drivers in a high-impedance state, and disables all the input buffers except the $\overline{S}$ input buffer. If this signal is not used, it must be connected to VDD.



Specifications

Monolithic 16 Mb family of products	16 Mb SRAM single chip die are organized in either a 2M x 8 or 512K x 32 format, packaged in an 86-lead ceramic flatpack

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