http://www.cubesatkit.com/

# CubeSat Kit™

## Pluggable Processor Module (PPM) B1

Hardware Revision: A

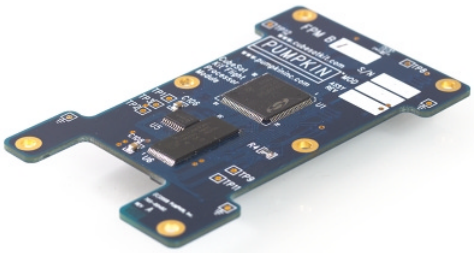
**PPM with Silicon Labs® C8051 for CubeSat Kit Motherboard**

### Applications

- CubeSat nanosatellite control, C&DH, TT&C
- General-purpose low-power computing for CubeSat Kit architecture
- Remote sensing for harsh environments

### Features

- For CubeSat Kit Motherboard (MB)
- Silicon Labs® C8051F120 8-bit microcontroller (MCU)
- 128KB program memory, 8448B on-chip SRAM
- Up to 100MIPS @ 100MHz
- Integrated peripherals:
  - 2 UARTs, 1 SPI, 1 I2C
  - 8-channel 8-bit 500ksps ADC
  - 2-channel 12-bit DAC
  - 5 16-bit counter/timers
  - 6 16-bit capture/compare modules
  - 2 analog comparators
  - WDT, JTAG, BOD, etc.
- On-board fast 128KB static RAM for XRAM
- Provision for external clock crystal
- Independent latchup (device overcurrent) protection
- Independent external reset supervisor (POR/BOR)
- Large-size PPM footprint
- 4-layer gold-plated blue-soldermask PCB
- Compatible with Pumpkin's Salvo™ RTOS and HCC-Embedded's EFFS-THIN SD Card file FAT file system for ease of programming



### ORDERING INFORMATION

Pumpkin P/N 710-00487

| Option Code | PPM Connector Height |
|---|---|
| /00 (standard) | +3mm |

Contact factory for availability of optional configurations. Option code /00 shown.

**CAUTION**

Electrostatic Sensitive Devices

Handle with Care

**CHANGELOG**

| Rev. | Date | Author | Comments |
|---|---|---|---|
| A | 20090728 | AEK | Initial revision. |
| B | 20090807 | AEK | Added photo. |

## OPERATIONAL DESCRIPTION

PPM B1 enables CubeSat Kit customers to utilize the C8051 processor on a CubeSat Kit Motherboard (MB). PPM B1 uses the 100-pin C8051F120-GQ, with a wide selection of on-chip peripherals. Additionally, a 1Mbit external static RAM is present for off-chip storage.

## ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Value | Units |
|---|---|---|---|
| Operating temperature | $T_A$ | -40 to +85 | ºC |
| Operating temperature, C8051F120 alone | $T_{A\_MCU}$ | -55 to +125 | ºC |
| Voltage on **+5V_USB** bus | | -0.3 to +6.0 | V |
| Voltage on **+5V_SYS** bus | | | |
| Voltage on **–FAULT_OC** open-collector output | | | |
| Voltage on **VCC** bus | | -0.3 to +3.6 | V |
| Voltage on **VCC_SD** bus | | | |
| Voltage on any processor pin except VDD and port I/O | | -0.3 to (**VCC** + 0.3) | V |
| Voltage on any processor VDD or port I/O pin | | -0.3 to +5.8V | V |
| Maximum current sourced or sunk by any processor port I/O pin | | 100 | mA |
| DC current through any pin of PPM connector **H1** | $I_{PIN\_MAX}$ | 1.2 | A |

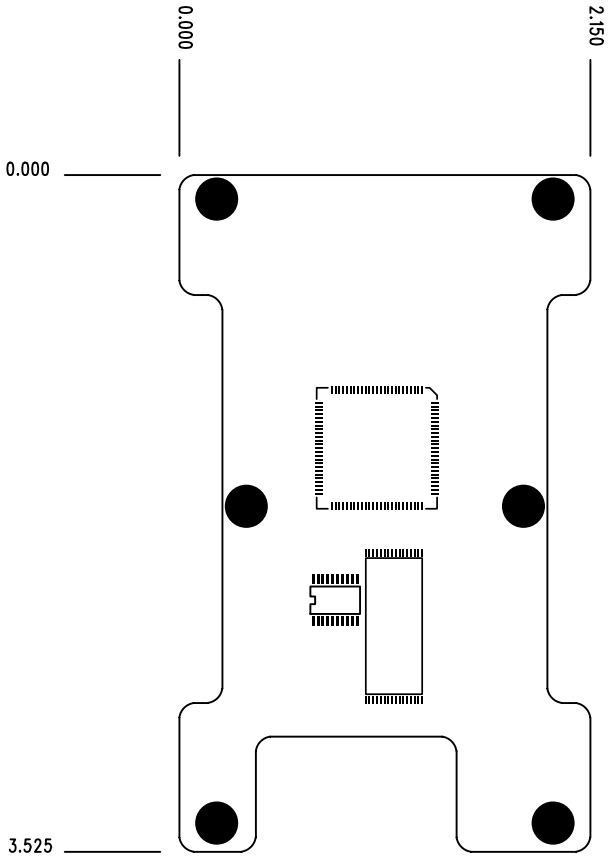
Refer to the C8-51F120/1/2/3/4/5/6/7 family datasheet for additional absolute maximum ratings associated with processor **U1**.

## PHYSICAL CHARACTERISTICS

| Parameter | Conditions / Notes | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Mass | | | | 16 | | g |
| Height of components above PCB | | | | | 2 | mm |
| Height of components below PCB[1] | | | | | 4 | mm |
| PCB width | Medium-size PPM | | | 54.6 | | mm |
| PCB length | | | | 89.5 | | mm |
| PCB thickness | | | | 1.6 | | mm |

## SIMPLIFIED MECHANICAL LAYOUT [2]

PPM B1 is implemented on a medium-size PPM PCB, as shown below.




[1] Not including connector H1.
[2] Dimensions in inches.

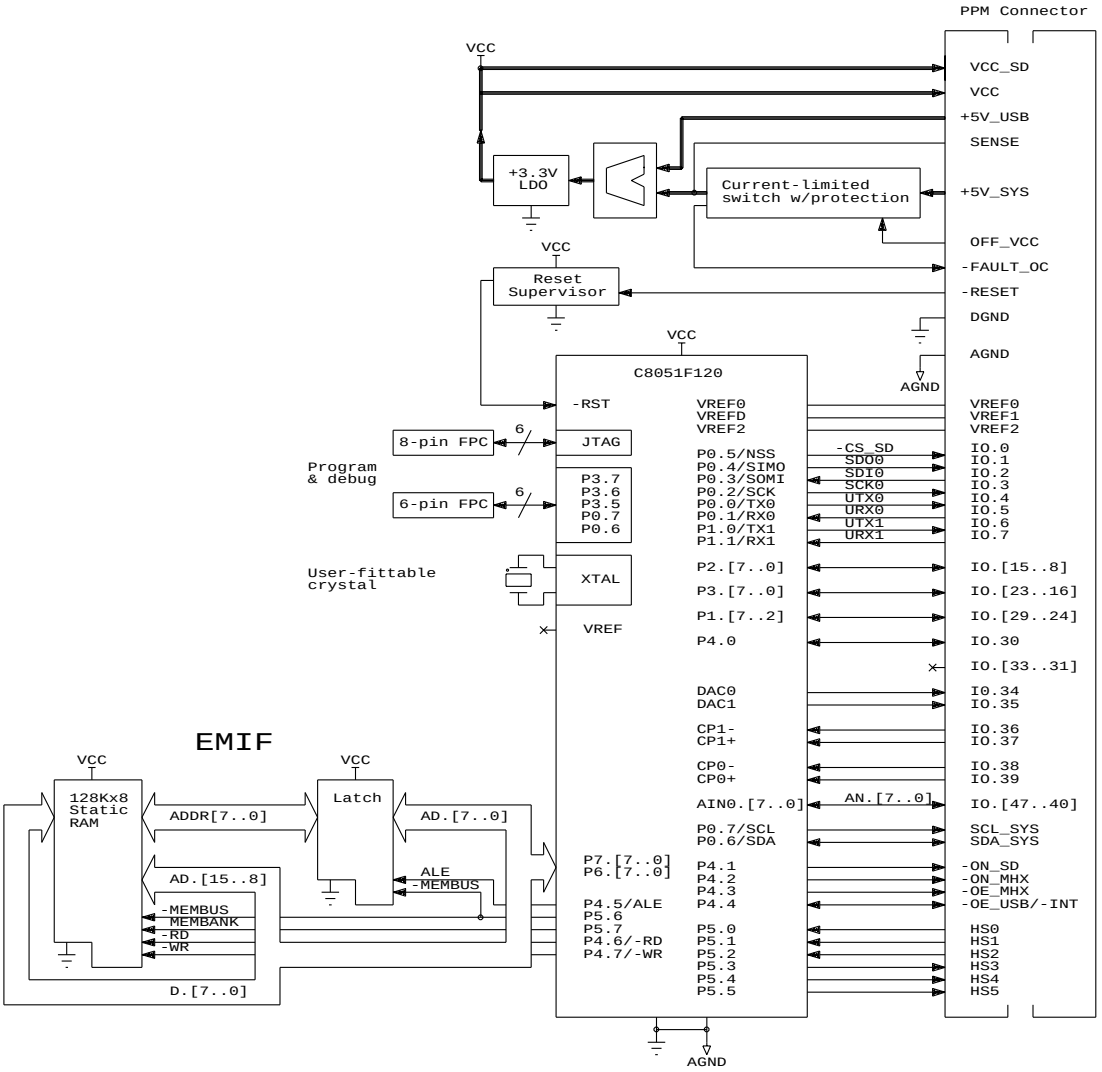
## ELECTRICAL CHARACTERISTICS

(T = 25ºC, +5V bus = +5V unless otherwise noted)

| Parameter | Conditions / Notes | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Reset voltage | **+5V_SYS** reduced until MCU resets | $V_{RESET\_MAX}$ | | | 3.1 | V |
| Operating Voltage | | $V_{CC}$ | | 3.3 | | V |
| SD Card Voltage | | $V_{CC\_SD}$ | | 3.3 | | V |
| Operating current | Typical operation | $I_{OP}$ | | TBD | | mA |
| | All control outputs inactive, PPM asleep | $I_{SLEEP}$ | | TBD | TBD | µA |
| Overcurrent trip point for **VCC** | Set by **R3** | $I_{TRIP\_VCC}$ | | 220 | | mA |
| Time to switch between **+5V_SYS** and **+5V_USB** power sources | Automatic | | | | 1 | µs |

## BLOCK DIAGRAM

PPM B1 provides regulated and current-limited +3.3V power, an external POR/BOR reset supervisor, JTAG and user interfaces for programming and debugging, a provision for an external crystal, an external high-speed[3] 1Mbit static RAM, connections to 45 of 48 I/O pins of the PPM connector, dedicated MB control and radio handshaking signals, a single-point analog/digital ground, and a careful assignment of the C8051 peripherals to the PPM connector and CubeSat Kit bus. One of the C8051's 100 pins is not used.




[3] 45ns.

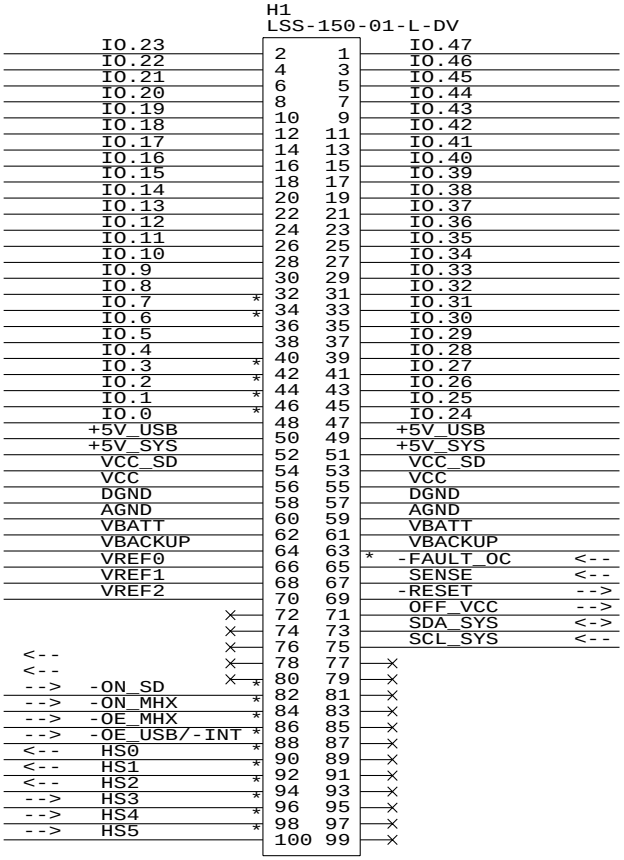
## PPM PIN DESCRIPTIONS

The PPM connector **H1** connects the PPM to resources residing on the MB and to resources accessible via the CubeSat Kit Bus connector.[4]

Those signals that are connected directly to the PPM connector and to the CubeSat Kit Bus connectors are tagged under the CSKB label below.[5] Signals marked with an '*' are associated with dedicated peripherals on the MB. They may also be used with off-board peripherals through the proper use of MB peripheral enables and MB power control.

The *potential* for a pin's function is described by the I/O field. The *recommended usage* (as a digital or analog input or output, or as a power pin) is listed in the Description field. I/O pins can generally be configured as general-purpose I/O if the recommended usage is not desired.

*Inputs* are signals *from* the MB *to* the PPM's processor **U1** or other circuitry. *Outputs* are signals *from* the PPM's processor **U1** or other circuitry *to* the MB.




[4] Not included. MBs are purchased separately from PPMs.

[5] The CubeSat Kit's system peripherals are numbered from 0 onwards (e.g., UART0, SPI0, etc.), and this nomenclature is used when referring to a PPM or CSK bus signal. The C8051's peripheral nomenclature begins with 0 (e.g., UART0, SMB0, etc.), and is used when referring to peripherals, signals and registers internal to the C8051.

## PPM PIN DESCRIPTIONS – I/O

| Name | Pin | I/O | CSKB | Description |
|---|---|---|---|---|
| **IO.0** | H1.48 | I/O | • | **-CS_SD**. Controls SD Card interface. From **P0.5** (**U1**.57). *Part of the MB's SD card interface. **P0.5** is normally configured as output function SPI0:NSS.* |
| **IO.1** | H1.46 | I/O | • | **SDO0**. SPI0 (master) data out. From **P0.4** (**U1**.58). *Part of the MB's SD card interface. **P0.4** is normally configured as output function SPI0:MOSI.* |
| **IO.2** | H1.44 | I/O | • | **SDI0**. SPI0 (master) data in. To **P0.3** (**U1**.59). *Part of the MB's SD card interface. **P0.3** is normally configured as input function SPI0:MISO.* |
| **IO.3** | H1.42 | I/O | • | **SCK0**. SPI0 clock. From **P0.2** (**U1**.60). *Part of the MB's SD card interface. **P0.2** is normally configured as output function SPI0:SCK.* |
| **IO.4** | H1.40 | I/O | • | **UTX0**. Tx0 data out. From **P0.0** (**U1**.62). ***P0.0** is normally configured as output function UART0:TX0.* |
| **IO.5** | H1.38 | I/O | • | **URX0**. Rx0 data in. To **P0.1** (**U1**.61). ***P0.1** is normally configured as input function UART0:RX0.* |
| **IO.6** | H1.36 | I/O | • | **UTX1**. Tx1 data out. From **P1.0** (**U1**.36). *Part of the MB's MHX/USB interface. **P1.0** is normally configured as output function UART1:TX1.* |
| **IO.7** | H1.34 | I/O | • | **URX1**. Rx1 data in. To **P1.1** (**U1**.35). *Part of the MB's MHX/USB interface. **P1.1** is normally configured as input function UART1:RX1.* |
| **IO.8** | H1.32 | I/O | • | General-purpose I/O. To/from **P2.0** (**U1**.46). |
| **IO.9** | H1.30 | I/O | • | General-purpose I/O. To/from **P2.1** (**U1**.45). |
| **IO.10** | H1.28 | I/O | • | General-purpose I/O. To/from **P2.2** (**U1**.44). |
| **IO.11** | H1.26 | I/O | • | General-purpose I/O. To/from **P2.3** (**U1**.43). |
| **IO.12** | H1.24 | I/O | • | General-purpose I/O. To/from **P2.4** (**U1**.42). |
| **IO.13** | H1.22 | I/O | • | General-purpose I/O. To/from **P2.5** (**U1**.41). |
| **IO.14** | H1.20 | I/O | • | General-purpose I/O. To/from **P2.6** (**U1**.40). |
| **IO.15** | H1.18 | I/O | • | General-purpose I/O. To/from **P2.7** (**U1**.39). |
| **IO.16** | H1.16 | I/O | • | General-purpose I/O. To/from **P3.0** (**U1**.54). |
| **IO.17** | H1.14 | I/O | • | General-purpose I/O. To/from **P3.1** (**U1**.53). |
| **IO.18** | H1.12 | I/O | • | General-purpose I/O. To/from **P3.2** (**U1**.52). |
| **IO.19** | H1.10 | I/O | • | General-purpose I/O. To/from **P3.3** (**U1**.51). |
| **IO.20** | H1.8 | I/O | • | General-purpose I/O. To/from **P3.4** (**U1**.50). |
| **IO.21** | H1.6 | I/O | • | General-purpose I/O. To/from **P3.5** (**U1**.49). |
| **IO.22** | H1.4 | I/O | • | General-purpose I/O. To/from **P3.6** (**U1**.48). |
| **IO.23** | H1.2 | I/O | • | General-purpose I/O. To/from **P3.7** (**U1**.47). |
| **IO.24** | H1.47 | I/O | • | General-purpose I/O. To/from **P1.2** (**U1**.34). |
| **IO.25** | H1.45 | I/O | • | General-purpose I/O. To/from **P1.3** (**U1**.33). |
| **IO.26** | H1.43 | I/O | • | General-purpose I/O. To/from **P1.4** (**U1**.32). |
| **IO.27** | H1.41 | I/O | • | General-purpose I/O. To/from **P1.5** (**U1**.31). |
| **IO.28** | H1.39 | I/O | • | General-purpose I/O. To/from **P1.6** (**U1**.30). |
| **IO.29** | H1.37 | I/O | • | General-purpose I/O. To/from **P1.7** (**U1**.29). |
| **IO.30** | H1.35 | I/O | • | General-purpose I/O. To/from **P4.0** (**U1**.98). |
| **IO.31** | H1.33 | I/O | • | Not connected. |
| **IO.32** | H1.31 | I/O | • | Not connected. |
| **IO.33** | H1.29 | I/O | • | Not connected. |
| **IO.34** | H1.27 | I/O | • | DAC voltage output. From **DAC0** (**U1**.100). |
| **IO.35** | H1.25 | I/O | • | DAC voltage output. From **DAC1** (**U1**.99). |
| **IO.36** | H1.23 | I/O | • | Comparator 1 inverting input. To **CP1-** (**U1**.6). |
| **IO.37** | H1.21 | I/O | • | Comparator 1 non-inverting input. To **CP1+** (**U1**.7). |

| | | | | |
|---|---|---|---|---|
| **IO.38** | H1.19 | I/O | • | Comparator 0 inverting input. To **CP0-** (**U1**.8). |
| **IO.39** | H1.17 | I/O | • | Comparator 0 non-inverting input. To **CP0+** (**U1**.9). |
| **IO.40** | H1.15 | I/O | • | **AN0**. Analog input 0. To **AIN0.0** (**U1**.18). |
| **IO.41** | H1.13 | I/O | • | **AN1**. Analog input 1. To **AIN0.1** (**U1**.19). |
| **IO.42** | H1.11 | I/O | • | **AN2**. Analog input 2. To **AIN0.2** (**U1**.20). |
| **IO.43** | H1.9 | I/O | • | **AN3**. Analog input 3. To **AIN0.3** (**U1**.21). |
| **IO.44** | H1.7 | I/O | • | **AN4**. Analog input 4. To **AIN0.4** (**U1**.22). |
| **IO.45** | H1.5 | I/O | • | **AN5**. Analog input 5. To **AIN0.5** (**U1**.23). |
| **IO.46** | H1.3 | I/O | • | **AN6**. Analog input 6. To **AIN0.6** (**U1**.24). |
| **IO.47** | H1.1 | I/O | • | **AN7**. Analog input 7. To **AIN0.7** (**U1**.25). |

## PPM PIN DESCRIPTIONS – Power

| Name | Pin | I/O | CSKB | Description |
|---|---|---|---|---|
| **+5V_USB** | H1.49<br>H1.50 | – | • | +5V USB power. From USB host. Powers PPM. |
| **+5V_SYS** | H1.51<br>H1.52 | – | • | +5V system power. From EPS or external +5V connector. Powers PPM. |
| **VCC_SD** | H1.53<br>H1.54 | – | | +3.3V SD Card power. From PPM's **VCC**. |
| **VCC** | H1.55<br>H1.56 | – | | +3.3V PPM power, MB power and I/O level. From PPM LDO **U4** using **+5V_SYS** and/or **+5V_USB**. |
| **DGND** | H1.57<br>H1.58 | – | • | Digital ground. |
| **AGND** | H1.59<br>H1.60 | – | • | Analog ground. |
| **VBATT** | H1.61<br>H1.62 | – | • | Not connected. |
| **VBACKUP** | H1.63<br>H1.64 | – | • | Not connected. |

## PPM PIN DESCRIPTIONS – Analog References

| Name | Pin | I/O | CSKB | Description |
|---|---|---|---|---|
| **VREF0** | H1.66 | – | • | ADC0 voltage reference input. To/from **VREF0** (**U1**.16). |
| **VREF1** | H1.68 | – | • | DAC voltage reference input.. To/from **VREFD** (**U1**.15). |
| **VREF2** | H1.70 | – | • | ADC2 voltage reference input. To/from **VREF2** (**U1**.17). |

## PPM PIN DESCRIPTIONS – Reserved

| Name | Pin | I/O | CSKB | Description |
|---|---|---|---|---|
| **RSVD0** | H1.72 | – | • | Not connected. Reserved for future use. |
| **RSVD1** | H1.74 | – | • | Not connected. Reserved for future use. |
| **RSVD2** | H1.76 | – | • | Not connected. Reserved for future use. |

## PPM PIN DESCRIPTIONS – MB-Specific

| Name | Pin | I/O | CSKB | Description |
|---|---|---|---|---|
| **CB4**<br>**USBDP** | H1.78 | I | | Not connected. |
| **CB2**<br>**USBDM** | H1.80 | I | | Not connected. |
| **-ON_SD** | H1.82 | O | | Control signal for SD Card power. From **P4.1** (**U1**.97). Active LOW, pulled high on the MB. When active, enables **VCC_CARD** on the MB, thereby powering SC Card socket and SD Card level translators / isolators. *Normally configured as a digital output.* |

| | | | | |
|---|---|---|---|---|
| **-ON_MHX** | H1.84 | O | | Control signal for MHX socket power. From **P4.2** (**U1**.96). Active LOW, pulled high on the MB. When active, enables **PWR_MHX** on the MB, thereby powering MHX socket and MHX level translators / isolators. *Normally configured as a digital output.* |
| **-OE_MHX** | H1.86 | O | | Control signal for MHX interface. From **P4.3** (**U1**.95). Active LOW, pulled high on the MB. When active, enables signals to pass through MHX level translators / isolators. *Normally configured as a digital output.* |
| **-OE_USB** | H1.88 | O | | Control signal for USB interface. From **P4.4** (**U1**.94). Active LOW, pulled high on the MB. When active, enables signals to pass through USB level translators / isolators. *Normally configured as a digital output.* |
| **-INT** | | I | | Output from RTC's -IRQ open-collector output. To **P4.4** (**U1**.94). Can be used to poll MB RTC's interrupt output. *Normally configured as a digital input.* |
| **HS0** | H1.90 | I | | Handshake signal. -RTS (USB) or -CTS (MHX). To **P5.0** (**U1**.88). *Can be configured as an external interrupt to **U1** or input handshake signal via its Peripheral Pin Select. Requires that **R10** be fitted on the MB.* |
| **HS1** | H1.92 | I | | Handshake signal. -DTR (USB) or -DSR (MHX). To **P5.1** (**U1**.87). *Can be configured as an external interrupt to **U1** or input handshake signal via its Peripheral Pin Select. Requires that **R11** be fitted on the MB.* |
| **HS2** | H1.94 | I | | Handshake signal. -PWE (USB) or -DCD (MHX). To **P5.2** (**U1**.86). *Can be configured as an external interrupt to **U1** or input handshake signal via its Peripheral Pin Select. Requires that **R12** be fitted on the MB.* |
| **HS3** | H1.96 | O | | Handshake signal. -CTS (USB) or -RTS (MHX). From **P5.3** (**U1**.85). *Can be configured as an output handshake signal via its Peripheral Pin Select. Requires that **R75** be fitted on the MB.* |
| **HS4** | H1.98 | O | | Handshake signal. -RI (USB) or -DTR (MHX). From **P5.4** (**U1**.84). *Can be configured as an output handshake signal via its Peripheral Pin Select. Requires that **R76** be fitted on the MB.* |
| **HS5** | H1.100 | O | | Handshake (reset) signal. -RST (USB) or -RST (MHX). From **P5.5** (**U1**.83). *Can be configured as an output handshake signal via its Peripheral Pin Select. Requires that **R77** be fitted on the MB.* |

## PPM PIN DESCRIPTIONS – Control & Status

| Name | Pin | I/O | CSKB | Description |
|---|---|---|---|---|
| **-FAULT_OC** | H1.65 | O | | Open-collector output from PPM's latchup prevention overcurrent switch. Active LOW. Wire-ORed to **-FAULT_OC** on the MB. |
| **SENSE** | H1.67 | – | • | Can be used to measure PPM's current consumption. The current used by the PPM from a single source is (source – **SENSE**) / 75mΩ. Depends on PPM implementation. |
| **-RESET** | H1.69 | I | • | Reset signal to PPM's reset supervisor. Active LOW. |
| **OFF_VCC** | H1.71 | I | • | Control signal to PPM's power circuit(s). Active HIGH. |

## PPM PIN DESCRIPTIONS – I2C Bus

| Name | Pin | I/O | CSKB | Description |
|---|---|---|---|---|
| **SDA_SYS** | H1.73 | I/O | • | I2C data. To/from **P0.6** (**U1**.56). *Part of the I2C interface. **P0.6** is normally configured as an I2C data input/output. Can also be used as general-purpose I/O.* |
| **SCL_SYS** | H1.75 | O | • | I2C clock. From **P0.7** (**U1**.55). *Part of the I2C interface. **P0.7** is normally configured as an I2C clock output. Can also be used as general-purpose I/O.* |

## PPM PIN DESCRIPTIONS – User-defined

| Name | Pin | I/O | CSKB | Description |
|---|---|---|---|---|
| **USER0** | H1.77 | I/O | • | Not connected. |
| **USER1** | H1.79 | I/O | • | Not connected. |
| **USER2** | H1.81 | I/O | • | Not connected. |
| **USER3** | H1.83 | I/O | • | Not connected. |
| **USER4** | H1.85 | I/O | • | Not connected. |
| **USER5** | H1.87 | I/O | • | Not connected. |
| **USER6** | H1.89 | I/O | • | Not connected. |
| **USER7** | H1.91 | I/O | • | Not connected. |
| **USER8** | H1.93 | I/O | • | Not connected. |
| **USER9** | H1.95 | I/O | • | Not connected. |
| **USER10** | H1.97 | I/O | • | Not connected. |
| **USER11** | H1.99 | I/O | • | Not connected. |

## XRAM INTERFACE

PPM B1 uses the C8051's External Memory Interface (EMIF) to provide an external 1Mbit (128Kx8) SRAM functioning as high-speed XRAM via a Cypress CY62128EV30 (**U6**).[6] A multiplexed interface is implemented via **U5** (SN74LVC373A) and **U6**. The 1Mbit SRAM is split into two selectable 64Kx8 pages. To use the EMIF, it must be configured to appear on the upper GPIO ports **P4**-**P7**, **–MEMBUS** must be active, and the desired bank must be selected via **MEMBANK**. Once configured,[7] the XRAM is accessed via the **MOVX** instruction, etc. The pin assignments associated with this interface are listed below.

## PIN DESCRIPTIONS – XRAM Interface

| Name | I/O | Description |
|---|---|---|
| **-MEMBUS** | O | Memory Bus Enable. From **P5.6** (**U1**.82). *To **U5**'s **–OE** pin and **U6**'s **–CE1** pin. When disabled (i.e., **-MEMBUS** is high), XRAM is not available, and is in its lowest-power state. When enabled, XRAM is available for full-speed operations.* |
| **MEMBANK** | O | Bank select. From **P5.7** (**U1**.81). *To **U6**'s **A16** pin. Selects between lower and upper 64Kx8 XRAM bank.* |
| **ALE** | O | Address Latch Enable. From **P4.5/ALE** (**U1**.93). *Part of **U1**'s EMIF on **P4**-**P7**. Latches the low-order bits of the multiplexed address EMIF address bus.* |
| **-RD** | O | Read strobe. From **P4.6/-RD** (**U1**.92). *Part of **U1**'s EMIF on **P4**-**P7**. To **U6**'s **–OE** pin.* |
| **-WR** | O | Write strobe. From **P4.7/-WR** (**U1**.91). *Part of **U1**'s EMIF on **P4**-**P7**. To **U6**'s **–WE** pin.* |
| **A[15..8]M** | O | Multiplexed (upper) address bits. From **P6[7..0]** (**U1**.[80..73]). *Part of **U1**'s EMIF on **P4**-**P7**. High-order address bits presented directly to **U6**'s **A[15..8]**.* |
| **AD[7..0]** | I/O | Multiplexed (lower) address and data bits. To/from **P7[7..0]** (**U1**.[72..65]). *Part of **U1**'s EMIF on **P4**-**P7**. Low-order address bits presented directly to latch **U5**'s **D[7..0]**, and data bits read back from **U6**'s **IO[7..0]**.* |

[6] Refer to the Cypress Semiconductor CY62128EV30 datasheet for more information.

[7] Wait states must be properly configured in U1 prior to accessing the XRAM.

## CONNECTORS

| Item | Description | Source | Part Number | Application |
|---|---|---|---|---|
| 1 | 100-pin, hermaphroditic | Samtec | LSS-150-01-L-DV | PPM connector (standard, +3mm) |

This connector information is provided for reference only.

## PROGRAMMING & DEBUGGING

PPM B1 provides one interface for programming and debugging – the popular and low-cost USB Debug Adapter from Silicon Devices. It provides another debugging adapter for simple user I/O. Both are implemented via Flexible Printed Circuit (FPC) connectors on the PPM.

8-pin FPC connector **J1** is for the USB Debug Adapter. Via Pumpkin's JFPC-C8051 adapter, customers can connect the USB Debug Adapter with its 10-pin 2x5 0.100" pitch dual-inline headers. The JFPC-C8051 connects to PPM B1 via an 8-conductor FPC cable.

6-pin FPC connector **J2** is for user debug purposes, and is compatible with 6-conductor FPC cables. Customers who wish to use the user port must fabricate their own adapter.[8] Its pin assignments are described below

## PIN DESCRIPTIONS – J2 User Debug Connector

| Pin | I/O | Description |
|---|---|---|
| **1** | I/O | **IO.23**. From **P3.7** (**U1**.47). *Can be used as general-purpose I/O.* |
| **2** | I/O | **IO.22**. From **P3.6** (**U1**.48). *Can be used as general-purpose I/O.* |
| **3** | I/O | **IO.21**. From **P3.5** (**U1**.49). *Can be used as general-purpose I/O.* |
| **4** | I/O | **SCL_SYS**. From **P0.7** (**U1**.55). *Normally used for an I2C monitor. Can be used as general-purpose I/O if properly configured.* |
| **5** | I/O | **SDA_SYS**. From **P0.6** (**U1**.46). *Normally used for an I2C monitor. Can be used as general-purpose I/O if properly configured.* |
| **6** | -- | Digital ground. |

## NOTES

Through the C8051's Priority Crossbar Decoder (XBAR) the user can enable digital peripherals and have them appear at certain I/O pins on **U1**. To be compatible with the CubeSat Kit Motherboard (MB), the UART0, SPI0 (4-wire mode), SMB0 and UART1 peripherals *must* be enabled in the XBAR. Enabling these four peripherals maps will cause their I/O to appear properly on **IO.[7..0]**, **SCL_SYS** and **SDA_SYS** (i.e., on the first 10 mappable C8051 I/O pins). Users are free to enable any of the other functions available through the XBAR, mapping them to **P1.2** or beyond.

N.B.: SPI0 *must* remain configured as 4-wire SPI, even if the Slave Select (NSS) functionality is not required. Configuring SPI0 for three-wire mode will map the **SCL_SYS**, **SDA_SYS**, **TX1** and **RX1** functions to the wrong pins of **U1**, the MB and the CubeSat Kit bus connector. Where NSS functionality is not required, **P0.5** can be treated as GPIO by appropriate register configuration.

**U1**'s **VREF** (Bandgap Voltage Reference Output) is left unconnected on Rev A of PPM B1. Future revisions may offer a user-fittable zero-ohm jumper from **VREF** to **VREF0**/**VREF2**/**VREFD**.

Crystal **X3** is not normally fitted, as the C8051F120 has an internal precision 24.5MHz clock source and PLL. Should the customer desire a different clock source, **X3** can be fitted.[9] Provisions for 0805-size loading caps **C3** and **C4** are included on the PPM B1 PCB.

[8] Alternatively, a Pumpkin JFPC-PIC24 programming adapter can be used, as it maps 6 FPC pins to a 6-pin 1x6 0.100" pitch single in-line header.
[9] E.g. ECS P/N ECS-xxx-20-5PXDN.

XRAM **U6** is not backed up by **VBACKUP** on Rev A of PPM B1. Future revisions may power **U6** through either **VCC** or **VBACKUP**.

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744 Naples Street
San Francisco, CA 94112 USA
tel: (415) 584-6360
fax: (415) 585-7948

web: http://www.pumpkininc.com/
email: info@pumpkininc.com

web: http://www.cubesatkit.com/
email: info@cubesatkit.com