NANOif (nano-if-2_custom)

NANOif Gen2 - Interface Control Document

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Approval of Document

	Name	Signature	Date
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Revision history

Last Edited Date	Revision Number	Status	Edited By	Pages / Paragraphs Affected	Change Ref
15/03/2018	0.1	Draft	DSE	All	Document Prepared
25/10/2018	1.0	Draft	DSE	All	Updated content
30/10/2018	1.1	Draft	DGA	All	Review
18/03/2020	1.2	Draft	DSE	All	Updated pinouts, removed old NANOif sketches
27/03/2020	1.3	Draft	DGA	P 12,13,14 / S 4.1.1	In Table 7 of P2 connector, RS422_1 interface pinout fixed and RS signal names renamed to RS422.
09/04/2020	1.4	Draft	DGA	S 4.1.1	Updated connector part number
11/05/2020	1.5	Draft	DSE	S 3.4	Added grounding scheme
04/06/2020	1.6	Draft	DSE	S 3.8.2	Added locations of thermal sensors
15/07/2020	1.7	Draft	DSE	S 4.1 S 6	Added explicit references to GPIO mapping Updated RS422 pinout. Updated Power and Signal Connector pin numbering. Updated CAN and LVDS shield numbering on pinout. Added schematics to electrical interfaces
22/07/2020	1.8	Draft	DSE	S 4.1	Updated connector descriptions
30/09/2020	1.9	Draft	DSE	S 4.1	Synchronized CAN bus names across SkyLabs product lines, added explicit reference to nominal/redundant bus.
23/12/2020	1.9.1	Draft	JHA	S 6.4 / S 4.1.2	Map ADC input pins with corresponding values in SW ICD
08/01/2021	1.10	Draft	DSE	S 3.3	Expanded inrush current chapter. Refined power consumption figures.

29/01/2021	1.11	Draft	NFE	S 3.7 S 3.8	Updated technical drawings and maximum envelope.
02/02/2021	1.12	Release	DGA	S 2.3	Consolidated technical specifications
12/02/2021	1.13	Release	NFE	S 2.3, S3.7	Updated mass, technical drawing and centre of mass.
02/04/2021	1.14	Release	NFE	S 3.8	Updated centre of mass and added MoI.

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1 Introduction

1.1 Scope

The following document provides the Interface Control Document for the NANOif (nano-if-2_custom), from hereinafter NANOif.

1.2 Applicable Documents

Applicable Documents identified in the following text are identified by AD-n, where “n” indicates the actual document, from the following list:

AD#	Title	Doc. No.	Issue	Date
AD1	NANOif Gen2 - Software Interface Control Document (SW ICD)		V1.7	30/03/2021

1.3 Reference Documents

Documents referenced in the following text, are identified by RD-n, where “n” indicates the actual document, from the following list:

RD#	Title	Doc. No.	Issue	Date
RD1	ROAD VEHICLES -- CONTROLLER AREA NETWORK (CAN) - PART 1: DATA LINK LAYER AND PHYSICAL SIGNALLING.	ISO Standard-11898-1		2013
RD2	PC/104-Plus Specification		Version 2.3	October 13, 2008

1.4 Acronyms and Abbreviations

AD	Applicable Documents
AR	Acceptance Review
BM	Breadboard Model
CCSDS	Consultative Committee for Space Data Systems
CDR	Critical Design Review
CLI	Command Line Interface
CoG	Centre of Gravity
COP	Communications Operations Procedure
CSP	Cost, Schedule, Performance
CTIA	Capacitive Trans Impedance Amplifier
DDJF	Design Development and Justification File
DDVP	Design Description and Verification Plan
EM	Engineering Model
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
EQM	Engineering Qualification Model
FARM	Frame Acceptance and Reporting Mechanism

FOV	Field of view
FS	Feasibility study
FWHM	Full Width at Half Maximum
IC	Integrated Circuit
ICD	Interface Control Document
JTAG	Joint Test Action Group
LEO	Low Earth Orbit
NIY	Not Implemented Yet
NVM	Non-Volatile Memory
PDR	Preliminary Design Review
PFM	Proto Flight Model
PRR	Preliminary Requirements Review
RD	Reference Documents
OBC	On-Board Computer
QR	Qualification Review
SNR	Signal to Noise Ratio
SRR	System Requirements Review
TBC	To Be Confirmed
TBD	To Be Determined
TBM	Test Bench Model
TOA	Time of Arrival
UART	Universal Asynchronous Receiver/Transmitter
WBS	Work Breakdown Structure
WP	Work Package

2 NANOif Overview

The NANOif interface board represents an integrated approach to support different dedicated systems in the context of the NANOsky I Platform. It provides the capability to interface all supported SkyLabs products with systems from other manufacturers. Its fault tolerance by design provides remarkable reliability and robustness against SEE. Fault tolerance is assured by redundancy on the component level and their flight heritage, latch-up protection by constant current monitoring and several mitigation techniques. The NANOif is fully compliant with the small foot-print PicoSkyFT™ soft-core processor, which furthermore increases operational reliability and delivers nearly 1 MIPS / MHz. NANOif features configurable interfaces, including the support for: ADC channels, GPIOs, UARTs, RS422s, SPIs, I2Cs, CAN and auxiliary CAN.

Figure 1: NANOif (nano-if-2) qualification model (QM)

2.1 Features

- Radiation hardened by design to increase reliability and robustness
  - Constant current monitoring and limiting
  - Selective components technology selection with flight heritage
  - EDAC protected memories/registers
  - Advance FDIR techniques
- Fully compliant design for PicoSkyFT™ processor
- SEE immune non-volatile MRAM memories for code and TM storage
- Instant boot up at power on
- Two clock sources available, including RTC
- Comprehensive local subsystem telemetry (currents, voltages, temperatures, etc.)
- PicoSkyFT™ programming and debugging interface
- Support for User connector and PC-104 Extension header
  - Hot/cold redundant CAN interface for TM/TC
  - 24 ADC channels with dedicated power interface
  - 5x RS422 interfaces
  - 28 GPIOs, 8 with interface remapping capability (SPI, I2C, UART)
  - Hot/cold redundant auxiliary CAN interface

2.2 Architecture overview

The NANOif hardware architecture is designed around the use of a PicoSkyFT softcore inside an ProASIC3 FPGA. The hardware includes two parallel MRAM memories (total of 4 Mbytes) for use as the program memory and uses an internal SRAM memory (total of 48 kbytes) for use as the data memory of the PicoSky core. Further, a SPI MRAM (total of 1 Mbyte) is present for storing critical system logs and other telemetry.

The NANOif exposes multiple different interfaces. First, two CAN drivers support interfacing the NANOif to a redundant CAN bus. And additional two CAN drivers are exposed on the Extension header. Additionally, five RS422 links are supported. The NANOif supports the monitoring of local telemetry through on-board ADCs. An additional 24 ADC channels are provided. Further, 28 GPIOs, 8 with remapping capability are also supported. A debug connector compliant with the PicoSkyLINK is present, exposing local debugging functionality. The PicoSkyFT SoC is clocked at 8 MHz.

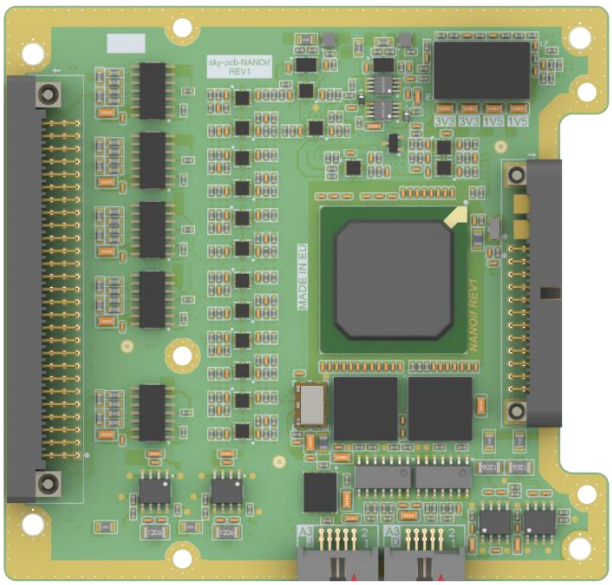

Figure 2: NANOif - Top

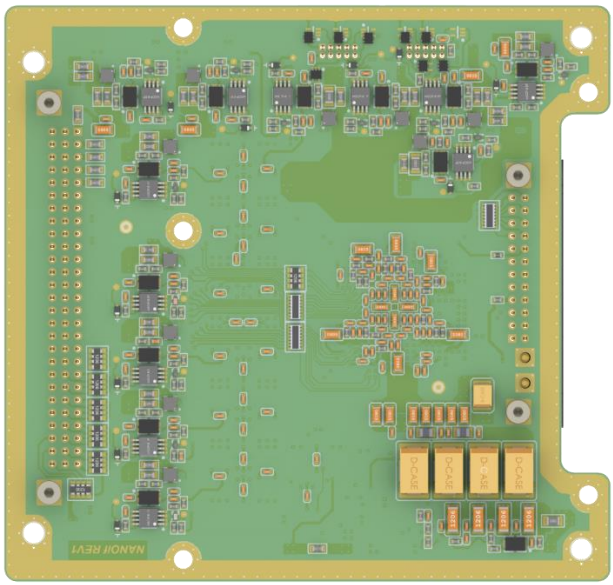

Figure 3: NANOif - Bottom

2.3 Technical specifications

Table 1: NANOif (nano-if-2) - Technical specification

	Description	Comment
Processor	PicoSkyFT-L SoC, running at 8MHz	Large memory model
On board memory		
Code memory	MRAM 4 MB (1Mb x 32-bit, unlimited read/write endurance, SEE immune)	EDAC protected
Data memory	Internal SRAM 48 kB	EDAC protected
TM storage	Serial MRAM 4 Mb (unlimited read/write endurance, SEE immune)	EDAC protected
On-board Communication interfaces	Redundant CAN bus for TM/TC	
Expansion Interfaces	2x CANaux bus 5x RS422 24x ADC 20x GPIO 8x GPIO with remap capability	Present on User connector and Extension header Possibility to use as UART, I2C, SPI
Supply voltage	5 V DC (+/- 10%)	For details refer to section 3.3.
Power consumption	< 1.25 W (typ)	For details refer to section 3.3.
Dimensions:	95 x 91 x 15 mm	For details refer to section 3.7.
Operation temperature	-10°C to +60°C	For details refer to section 3.9.1.
Storage temperature	-20°C to +65°C	For details refer to section 3.9.1.
Mass:	55 g	For details refer to section 3.8.

3 Module specifications and generic parameters

3.1 Primary Function and Description

The NANOif is designed to function as an interface extension subsystem of a nanosatellite. As such, it implements a PicoSkyFT core with sufficient amounts of program and data memory for even the most intensive interfacing tasks, while being compatible with the PC-104 form factor. It supports a hot redundant CAN bus interface as well as various interfaces over the User and Extension connector. It features extensive fault tolerant features, including the features built into the FT version of the PicoSky core, as well as integrated Latching Current Limiters and additional SoC protections (Watchdog timer, two CRC protected banks of program memory).

The NANOif system contains:

- ProASIC3 FPGA running PicoSkyFT (protected by LCL)..
- Protection of FPGA, power regulator and related circuitry by autonomous LCL.
- 2 x 16x1M MRAM as program memory (protected by LCL).
- Internal FPGA 48 kB SRAM as data memory.
- 4 Mbit SPI MRAM (protected by LCL).
- Hot redundant CAN interface (individually protected by LCL).
- 2 x high speed LVDS interface (protected by LCL).
- Debug interface.
- Local telemetry monitoring (Voltages, Temperatures).
- 24x external ADC channels
- 28x external GPIOs
- 5x RS422 interfaces
- 2x auxiliary CAN interface

The PicoSkyFT SoC design includes:

- PicoSkyFT core running at 8 MHz.
- LUT-based supervisor for protecting user program from errors.
- LUT-based program memory CRC check assuring valid code is running.
- A two-bank program memory architecture, allowing the running program to perform upgrades to the firmware in the other bank.
- Dedicated debug core exposed over the CAN network, allowing low-level access.
- DMA, NVIC, DIT, MPU, Scrubber controllers
- Timers
- UART, SPI, I2C controllers
- SPI-MRAM NVMEM controller
- CAN controllers
- LCL management peripheral with error injection capability for diagnostics.
- ADC peripheral
- Watchdog timer

3.2 Module Block Diagram

The NANOif design is focused that most hardware components are accessed using a dedicated SoC peripheral. The exception is the MRAM memory, which is connected directly to the PicoSky core via the memory controller. The following block diagram demonstrates the NANOif design.

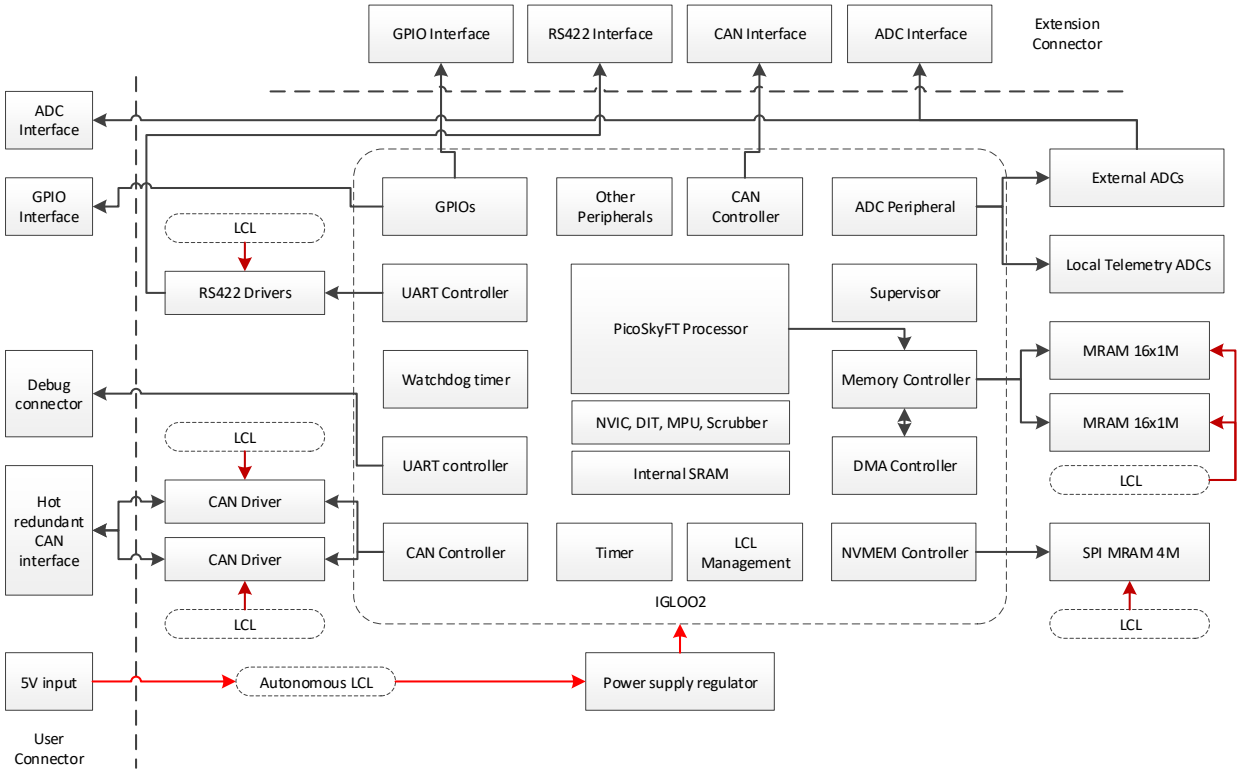

Figure 4: NANOif Basic block diagram

3.3 Electrical Power

NANOif shall be powered with 5V regulated power line. Other required NANOif voltages are generated internally with integrated DC-DC converters. Associated voltage ranges are 1.5V, 3.3V and 5V.

Values are given for one NANOif.

Table 2: NANOif Electrical characteristics

Num. of power interfaces:	1 (5 V, ±10%)
Voltage rails:	1.5 V, 3.3 V, 5 V

Table 3: NANOif Power consumption

Power consumption	At 25 °C	At -35 °C	At 70 °C
Nominal mode • All CAN channels terminated. • All RS422 channels terminated.	1.18 W	1.18 W	1.21 W

3.3.1 Inrush current profile

The inrush current of the NANOif is defined by the input capacitances of the NANOif local power supply DC-DC converters. There is no active inrush limiting circuitry present on the NANOif.

Table 4: NANOif Inrush current characteristics

Equivalent input capacitance	80 uF

Inrush profile (lead connected to 5V power supply, no soft start): • Inrush duration • Inrush peak	 35 us 20 A
Inrush charge transferred (0V to 5V)	0.40 mAs

3.3.2 Turn off/on procedure

The on/off procedure of NANOif is to switch on/off its power supply line and/or via on-board subsystem LCL where in case of a detected anomaly (excessive current draw) resets autonomously.

3.4 Grounding Scheme

The whole NANOif uses a single common ground topology. All parts of the NANOif share a common ground. All connector pins with the signal type marked as GND refer to this common ground potential.

Additional ground signal types are:

- CAN ground: connected to GND through a 0 Ohm resistor near the CAN driver.
- RS422 ground: connected to GND through a 0 Ohm resistor near the RS422 driver.
- LVDS shield: connected to GND through a 0 Ohm resistor near the LVDS driver.

3.5 Electro Static Discharge

The NANOif contains sensitive electronic components that are susceptible to be damaged by static electricity. When handling or installing the NANOif observe appropriate precautions and ESD safe practices.

3.6 Electromagnetic Compatibility

Each NANOif can be upon request RF characterised and tested for EMC, according to ECSS-E-ST-20-07C. Tests are performed in facility certified for CCA EMC test procedures.

3.7 Mechanical Interface Control Drawing

The NANOif is fully compliant to PC104 mounting specifications. For standard details please refer to RD2. NANOif electronics board is fixed into common PC/104 compliant fixation rod. Cable stripes are used to provide power and establish communication link between NANOif and other command and data handling equipment, over CAN interfaces.

Please take special care when designing mechanical stack up, to keep clear of exposed components of the NANOif subsystem. It is recommended to provide a clearance between this and another component in stack up of at least 2 mm on top and bottom.

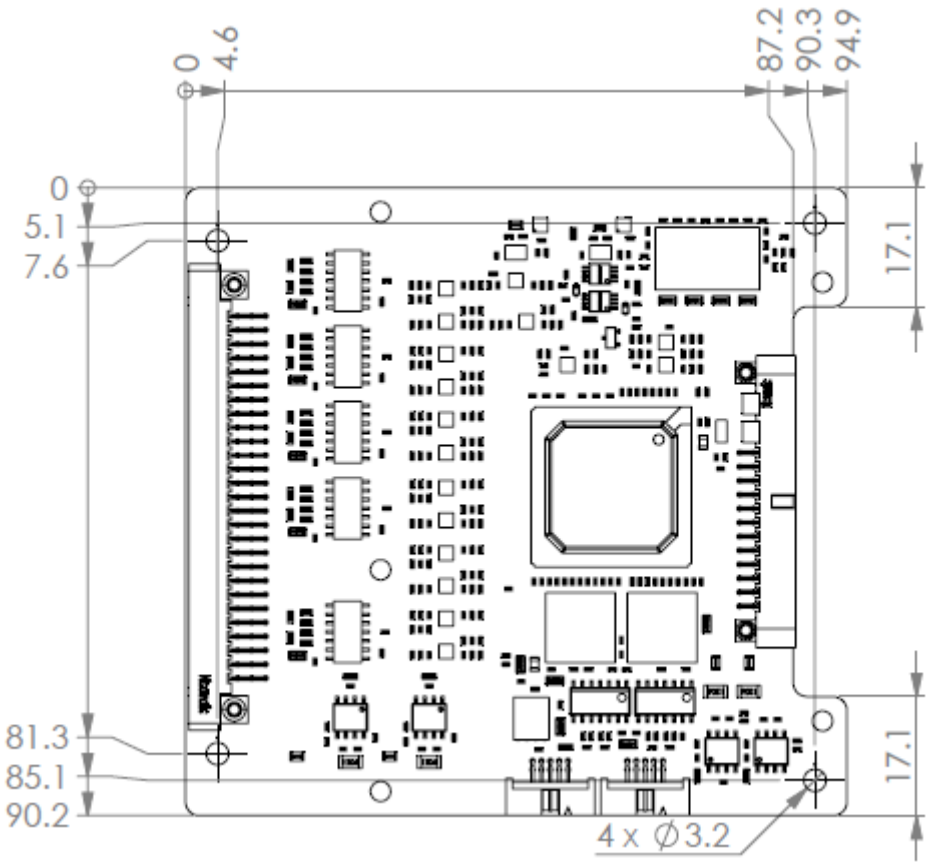

Figure 5: Mechanical Drawing of NANOif – Top view

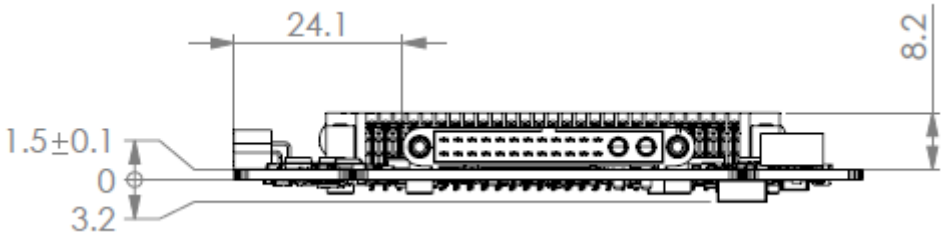

Figure 6: Mechanical Drawing of NANOif – Front view

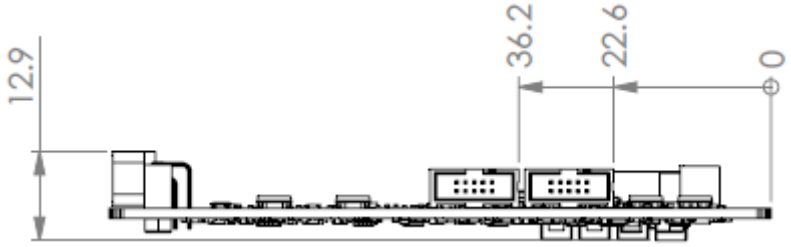

Figure 7: Mechanical Drawing of NANOif – Side view

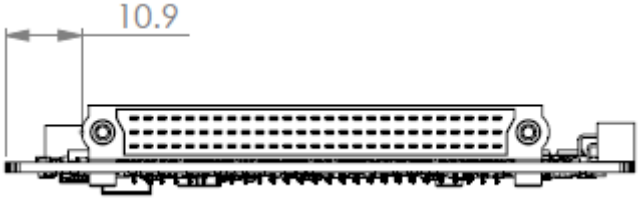

Figure 8: Mechanical Drawing of NANOif – Back view

3.8 Mechanical Interface Control parameters

NANOif mechanical properties:

Table 5: NANOif mechanical properties:

Dimensions:	90.2 x 94.9 x 12.9 mm (110.42cm³)
Mass:	54.00 g (PCB, components) – unmargined 55.05 g (PCB, components) – 5% margined

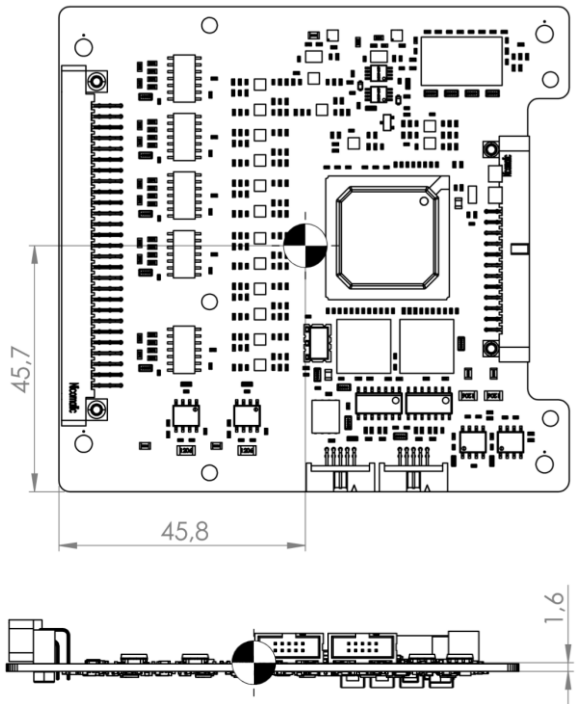

Figure 9: Centre of mass

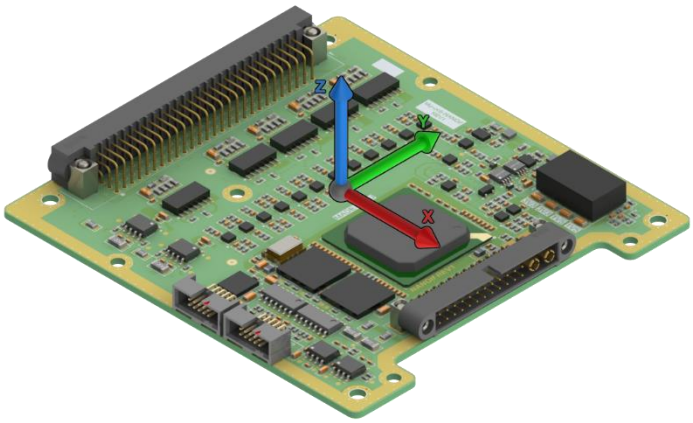

Figure 10: Reference coordinate system

Moments of inertia: (grams * square millimeters)

Taken at the centre of mass (Figure 9**Error! Reference source not found.**) and aligned with the output coordinate system (Figure 10).

Table 6: NANOif moments of Inertia

Lxx = 34901.14	Lxy = 1519.99	Lxz = -384.02
Lyx = 1519.99	Lyy = 41682.79	Lyz = -24.58
Lzx = -384.02	Lzy = -24.58	Lzz = 76133.35

3.8.1 Materials specifications

Material	Manufacturer	%TML	%CVCM	%WVR	Application	Note
PCB material	ISOLA 370HR			0.15	PCB board	ECSS identified
Solder	SAC305				Soldering	

3.8.2 List and location of thermal sensors

Sensor	Name	Type	PCB location
T1	FPGA Sensor	External NTC (B=3380)	Top
T2	Regulator Sensor	Internal Sensor of Power Regulator	Top

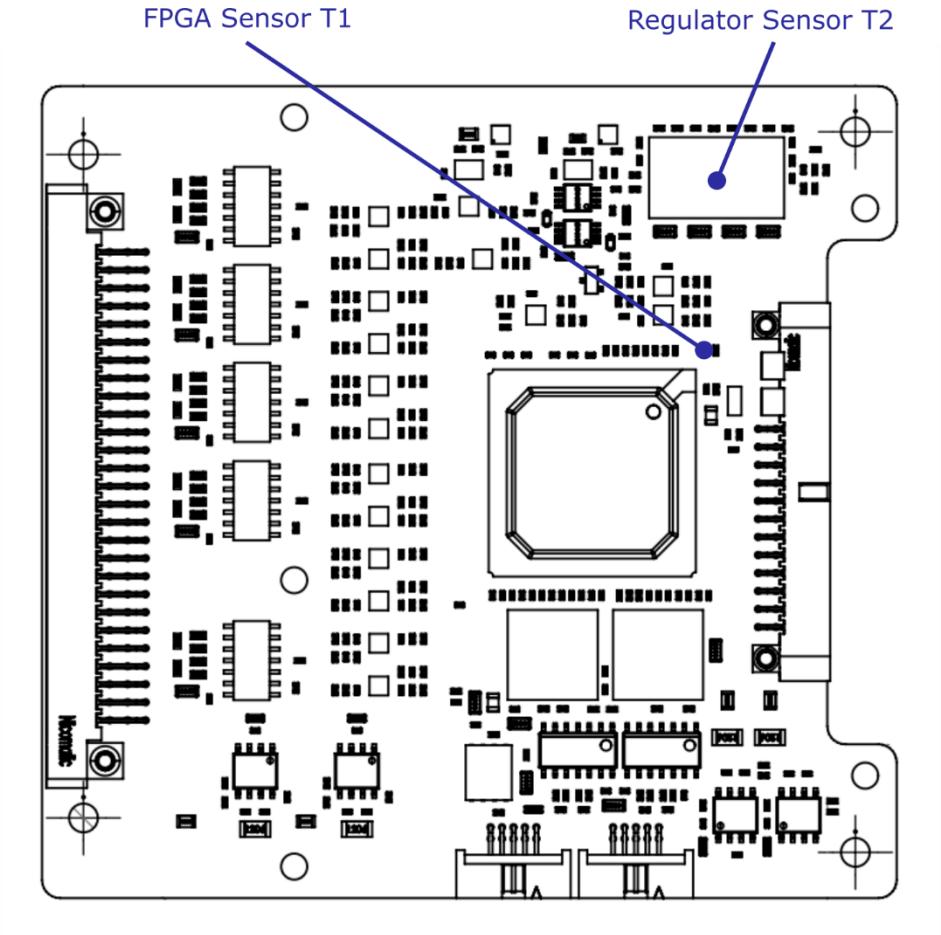

Figure 11: Location of NANOif Thermal Sensors

3.9 Environmental Requirements

3.9.1 Thermal Limits

Table below describes the thermal limits for the NANOif. Recommended values for all electronic modules are provided in the table.

The definition of the Design, Acceptance and Qualification limits are as follows:

- **Design Temperature**: The temperature to which the flight equipment can operate in service and work satisfactorily.
- **Qualification Temperature**: The temperature to which the module design has been tested and proven to work satisfactorily.
- **Acceptance Temperature**: The temperature to which the flight equipment has been tested and proven to work satisfactorily.

Table 7: Temperature Limits

	Qualification	Acceptance	Design
Non-operating temperature limits	-30°C - +75°C	-25°C - +70°C	-20°C - +65°C
Start-up temperature limits	-35°C - +70°C	-30°C - +65°C	-25°C - +60°C
Operating temperature limits	-20°C - +70°C	-15°C - +65°C	-10°C - +60°C

3.9.2 Thermal Dissipation

This section provides information on the thermal dissipation of the NANOif modules, in Watts.

Thermal dissipation will be less than estimated power consumption for each module.

Table 8: NANOif Power Dissipation

	Power Dissipation [W]	Primary thermal path
NANOif	< 1.2 W	To PCB fixation holes

3.9.3 Definition of External Surface Properties

NANOif module is not incorporated into any enclosure.

4 Harness

NANOif provides power and separate communication interfaces connector.

4.1 NANOif connectors

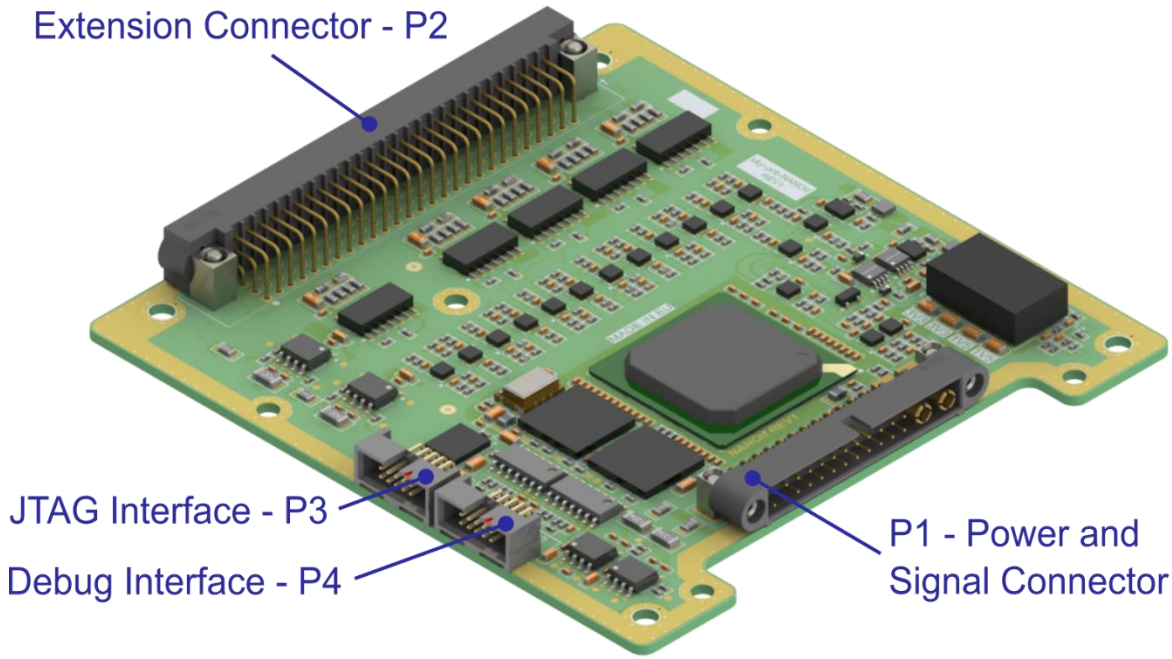

Figure 12: NANOif connector designators

4.1.1 Power and Signal Connector

Connector name:	**NANOif Power and Signal connector**
Connector designator:	**P1**
Connector function:	**Power supply and communication interface**
Connector type:	**Multi-mix connector, power and signal to the Board, MALE**
Connector part number:	**221V24F26-0200-3400CMM**
Mate connector part number:	**222S24M16-0200-4310**

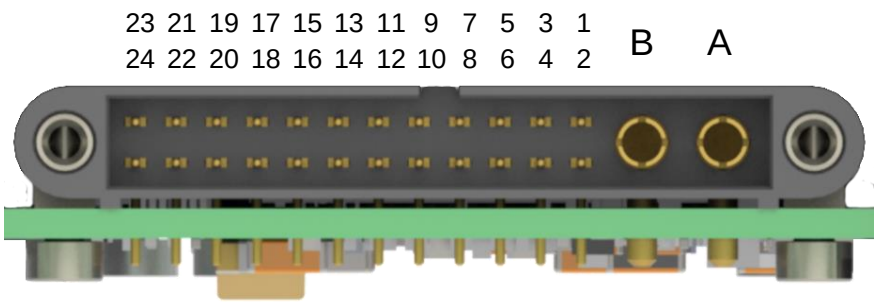

Figure 13: NANOif Power and Signal Connector (221V24F26-0200-3400CMM)

Table 9: NANOif Power and Signal connector pins (221V24F26-0200-3400CMM)

Pin	Signal Name	Signal Type	Wire Type	Notes
A	Power +5V	+5 V power supply	AWG-16	
B	Power GND	GND	AWG-16	
1	CANB_P	CAN signal level	AWG-26	Redundant bus
2	CANB_N	CAN signal level	AWG-26	Redundant bus
3	CANB GND	CAN ground	AWG-26	Redundant bus
4	CANA GND	CAN ground	AWG-26	Nominal bus
5	CANA_P	CAN signal level	AWG-26	Nominal bus
6	CANA_N	CAN signal level	AWG-26	Nominal bus
7	LVDS1_SHD	LVDS TX cable shield	AWG-26	
8	LVDS0_TX_P	LVDS signal level	AWG-26	
9	LVDS1_TX_P	LVDS signal level	AWG-26	
10	LVDS0_TX_N	LVDS signal level	AWG-26	
11	LVDS1_TX_N	LVDS signal level	AWG-26	
12	LVDS0_RX_N	LVDS signal level	AWG-26	
13	LVDS1_RX_N	LVDS signal level	AWG-26	
14	LVDS0_RX_P	LVDS signal level	AWG-26	
15	LVDS1_RX_P	LVDS signal level	AWG-26	
16	LVDS0_SHD	LVDS TX cable shield	AWG-26	
17	GPIO7	GPIO	AWG-26	GPIO0_7
18	GPIO6	GPIO	AWG-26	GPIO0_6
19	GPIO5	GPIO	AWG-26	GPIO0_5
20	GPIO4	GPIO	AWG-26	GPIO0_4
21	GPIO3	GPIO	AWG-26	GPIO0_3
22	GPIO2	GPIO	AWG-26	GPIO0_2
23	GPIO1	GPIO	AWG-26	GPIO0_1
24	GPIO0	GPIO	AWG-26	GPIO0_0

4.1.2 Extension connector

Connector name: **NANOif Extension connector**

Connector designator: **P2**

Connector function: **Extension connector**

Connector type: **Multi-mix connector, signal to the Board, MALE**

Connector part number: **321V081F51**

Mate connector part number: **322S081H01**

27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32 31 30 29 28
81 80 79 78 77 76 75 74 73 72 71 70 69 68 67 66 65 64 63 62 61 60 59 58 57 56 55

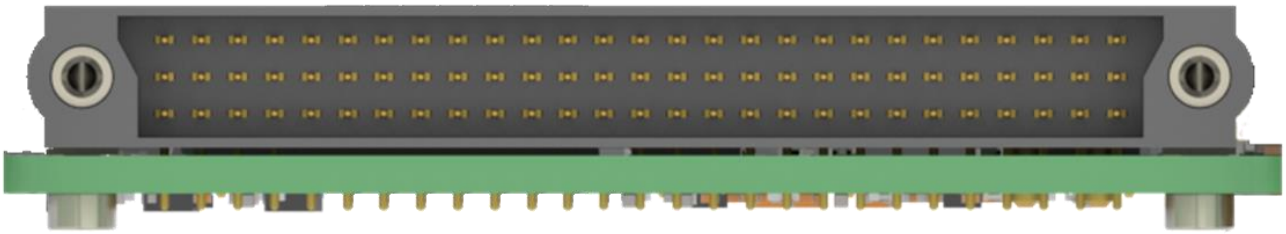

Figure 13: NANOif Extension Connector (321V081F51)

Table 10: NANOif Extension Connector pins (321V081F51)

Pin	Signal Name	Signal Type	Wire Type	Notes
1	RS422_1 GND	RS422 ground	AWG-26	
2	RS422_2 GND	RS422 ground	AWG-26	
3	RS422_3 GND	RS422 ground	AWG-26	
4	RS422_4 GND	RS422 ground	AWG-26	
5	RS422_5 GND	RS422 ground	AWG-26	
6	CANaux1 GND	CAN ground	AWG-26	
7	CANaux0 GND	CAN ground	AWG-26	
8	CANaux1_N	CAN signal level	AWG-26	
9	CANaux1_P	CAN signal level	AWG-26	
10	CANaux0_N	CAN signal level	AWG-26	
11	CANaux0_P	CAN signal level	AWG-26	
12	GND	GND	AWG-26	
13	GPIOB19	GPIO	AWG-26	GPIO3_2
14	GPIOB18	GPIO	AWG-26	GPIO3_1
15	GPIOB15	GPIO	AWG-26	GPIO2_6
16	GPIOB12	GPIO	AWG-26	GPIO2_3
17	GPIOB9	GPIO	AWG-26	GPIO2_0
18	GPIOB6	GPIO	AWG-26	GPIO1_5
19	GPIOB3	GPIO	AWG-26	GPIO1_2
20	ADCIN_122	ADC signal level	AWG-26	ADC ch. 24 *
21	ADCIN_111	ADC signal level	AWG-26	ADC ch. 11 *

22	ADCIN_092	ADC signal level	AWG-26	ADC ch. 21 *
23	ADCIN_081	ADC signal level	AWG-26	ADC ch. 08 *
24	ADCIN_062	ADC signal level	AWG-26	ADC ch. 18 *
25	ADCIN_051	ADC signal level	AWG-26	ADC ch. 05 *
26	ADCIN_032	ADC signal level	AWG-26	ADC ch. 15 *
27	ADCIN_021	ADC signal level	AWG-26	ADC ch. 02 *
28	RS422_1_TXN	RS422 signal level	AWG-26	
29	RS422_1_TXP	RS422 signal level	AWG-26	
30	RS422_3_TXP	RS422 signal level	AWG-26	
31	RS422_3_RXN	RS422 signal level	AWG-26	
32	RS422_5_TXN	RS422 signal level	AWG-26	
33	RS422_5_RXN	RS422 signal level	AWG-26	
34	RS422_4_RXN	RS422 signal level	AWG-26	
35	RS422_4_TXP	RS422 signal level	AWG-26	
36	RS422_2_TXN	RS422 signal level	AWG-26	
37	RS422_2_RXP	RS422 signal level	AWG-26	
38	GND	GND	AWG-26	
39	GND	GND	AWG-26	
40	GPIOB20	GPIO	AWG-26	GPIO3_3
41	GPIOB17	GPIO	AWG-26	GPIO3_0
42	GPIOB14	GPIO	AWG-26	GPIO2_5
43	GPIOB11	GPIO	AWG-26	GPIO2_2
44	GPIOB8	GPIO	AWG-26	GPIO1_7
45	GPIOB5	GPIO	AWG-26	GPIO1_4
46	GPIOB2	GPIO	AWG-26	GPIO1_1
47	ADCIN_121	ADC signal level	AWG-26	ADC ch. 12 *
48	ADCIN_102	ADC signal level	AWG-26	ADC ch. 22 *
49	ADCIN_091	ADC signal level	AWG-26	ADC ch. 09 *
50	ADCIN_072	ADC signal level	AWG-26	ADC ch. 19 *
51	ADCIN_061	ADC signal level	AWG-26	ADC ch. 06 *
52	ADCIN_042	ADC signal level	AWG-26	ADC ch. 16 *
53	ADCIN_031	ADC signal level	AWG-26	ADC ch. 03 *
54	ADCIN_012	ADC signal level	AWG-26	ADC ch. 13 *
55	RS422_1_RXP	RS422 signal level	AWG-26	

56	RS422_1_RXN	RS422 signal level	AWG-26	
57	RS422_3_TXN	RS422 signal level	AWG-26	
58	RS422_3_RXP	RS422 signal level	AWG-26	
59	RS422_5_TXP	RS422 signal level	AWG-26	
60	RS422_5_RXP	RS422 signal level	AWG-26	
61	RS422_4_RXP	RS422 signal level	AWG-26	
62	RS422_4_TXN	RS422 signal level	AWG-26	
63	RS422_2_TXP	RS422 signal level	AWG-26	
64	RS422_2_RXN	RS422 signal level	AWG-26	
65	GND	GND	AWG-26	
66	3V3_EXT	3.3V Output for ADC	AWG-26	
67	GND	GND	AWG-26	
68	GPIOB16	GPIO	AWG-26	GPIO2_7
69	GPIOB13	GPIO	AWG-26	GPIO2_4
70	GPIOB10	GPIO	AWG-26	GPIO2_1
71	GPIOB7	GPIO	AWG-26	GPIO1_6
72	GPIOB4	GPIO	AWG-26	GPIO1_3
73	GPIOB1	GPIO	AWG-26	GPIO1_0
74	ADCIN_112	ADC signal level	AWG-26	ADC ch. 23 *
75	ADCIN_101	ADC signal level	AWG-26	ADC ch. 10 *
76	ADCIN_082	ADC signal level	AWG-26	ADC ch. 20 *
77	ADCIN_071	ADC signal level	AWG-26	ADC ch. 07 *
78	ADCIN_052	ADC signal level	AWG-26	ADC ch. 17 *
79	ADCIN_041	ADC signal level	AWG-26	ADC ch. 04 *
80	ADCIN_022	ADC signal level	AWG-26	ADC ch. 14 *
81	ADCIN_011	ADC signal level	AWG-26	ADC ch. 01 *

* ADC channel numbers correspond to NANOif User ADC TMs (19 – 24) defined in SW ICD.

5 Telecommands and Telemetry

The primary access mechanism for the telecommands and the telemetry of the NANOif subsystem is through the CAN interface. The details of the telecommands and telemetry can be found in [AD1].

6 Interfaces - Electrical Characteristics

6.1 CAN Interface

Controller–area network (CAN or CAN-bus) is an automotive bus standard designed to allow microcontrollers and devices to communicate with each other within a vehicle without a host computer. CAN is a message-based protocol, designed specifically for automotive applications but is now also used in other areas, such as industrial automation, medical equipment, and for space applications.

CAN is a multi-master broadcast serial bus standard for connecting Electronic Control Units (ECUs). Each node is able to send and receive messages, but not simultaneously. A message consists primarily of an id, which represents the priority of the message, and up to eight data bytes. It is transmitted serially onto the bus. This signal pattern is encoded in Non-Return-to-Zero (NRZ) and is sensed by all nodes.

The devices that are connected by a CAN network are typically sensors, actuators, and other control devices. These devices are not connected directly to the bus, but through a host processor and a CAN controller.

If the bus is free, any node may begin to transmit. If two or more nodes begin sending messages at the same time, the message with the more dominant ID (which has more dominant bits, i.e., zeroes) will overwrite other nodes' less dominant ID's, so that eventually (after this arbitration on the ID) only the dominant message remains and is received by all nodes. This mechanism is referred to as priority-based bus arbitration. Messages with numerically smaller values of ID have higher priority and are transmitted first.

NANOif TM/TC is based on CAN Specification (RD1), Version 2 Bosch GmbH – CAN standard B, 29-bit Identifier, at the application layer the CAN-TS protocol is delivered, developed by SkyLabs.

The CAN standard requires that the CAN bus is terminated at each end by a one-hundred-and-twenty-ohm (120 Ohm) resistor. It is possible that the termination resistors are fitted in the harness/connector and not in the module.

6.1.1 CAN Physical Interface

6.1.1.1 CAN Physical Interface electrical specifications

Table 11: CAN Interface electrical specifications

Parameter	Minimum	Typical	Maximum
Maximum DC voltage	-58V	N/A	58V
Maximum transient voltage	-150V	N/A	100V
Maximum current	-40mA	N/A	100mA
ESD discharge (HBM) *	- 8kV	N/A	+8kV
ESD discharge (IEC 61000-4-2) *	- 8kV	N/A	+8kV
* Discharge at available pins CANH and CANL on connector			

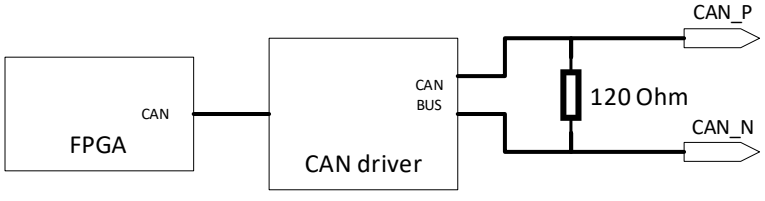

Figure 13: CAN schematic (note: 120 Ohm termination resistor optional)

6.1.2 CAN Redundancy Operation

NANOif support communication over cold or hot redundant CAN busses. In case hot redundant networking topology is not considered in satellite, hot redundant operation can be disabled.

Hot redundant operation means that transmitting CAN node transmits single frame throughout both CAN busses concurrently. Receiving CAN nodes are listening on both CAN busses, where receiving CAN arbiter selects bus, on which the CAN frame arrived first. In case of detecting concurrent reception, arbiter always select primary CAN bus (CAN_A).

6.2 RS422 Interface

To enable interfacing with other satellite subsystems or equipment, the NANOif supports up to 4 RS422 compatible communication interfaces. The differential drivers and receivers used meet or exceed the requirements of the ANSI TIA/EIA-422 standard.

6.2.1 RS422 Physical Interface

The RS422 interface can provide data rates up to 20Mbps while bus-terminal ESD exceeds 16 kV and operates in wide temperature range. Selected RS422 physical driver is intended for use in simplex or distributed simplex bus structures, while also supporting more advanced configuration options. The driver enable function puts the differential outputs into a high-impedance state.

6.2.1.1 RS422 electrical specifications

Table 12: RS422 driver electrical specifications

Parameter	Minimum	Typical	Maximum
Steady-state differential output voltage	1.5 V	2.3 V	N/A
Change between differential output voltage	-0.2 V	N/A	+0.2 V
Steady-state common-mode output voltage	1.6 V	N/A	2.3 V
Change in common-mode output voltage	50 mV	N/A	50 mV
Peak to peak common-mode output voltage	NA	0.5 V	NA

Table 13: RS422 receiver electrical specifications

Parameter	Minimum	Typical	Maximum
Positive-going differential input voltage threshold	NA	NA	-20 mV
Negative-going differential input voltage threshold	-200 mV	NA	NA

High level output voltage	2.4 V	NA	NA
Low level output voltage	NA	NA	0.4 V
Hysteresis	NA	50 mV	0.4 V

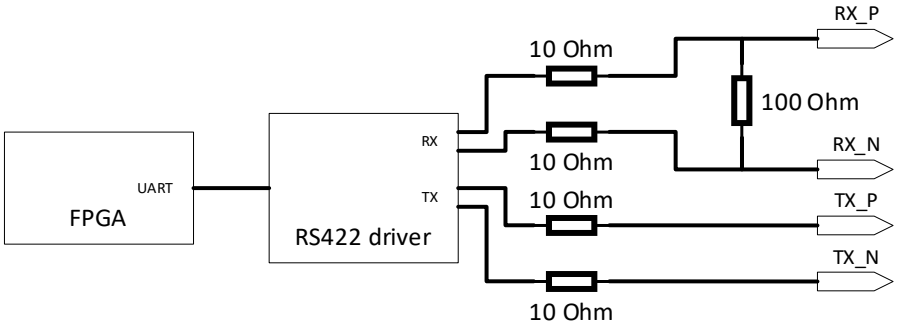

Figure 13: RS422 schematic

6.3 GPIO Interface

The GPIO interfaces feature general purpose I/Os with I/O remapping capability (capability to use GPIO pins for alternative functions, such as PWM, UART, I2C, SPI, etc.). The GPIO interface follows the LVCMOS 3.3V standard.

All GPIO pins are connected to FPGA I/O pins, with a 10 Ohm resistor in series.

Table 14: GPIO interface electrical specifications

Parameter	Minimum	Typical	Maximum
Input current	N/A	N/A	10 uA
DC Input High	2.0 V	N/A	3.45 V
DC Input Low	-0.3 V	N/A	0.8 V
Output current	N/A	N/A	12 mA
DC Output High	2.9 V	N/A	3.3 V
DC Output Low	0.0 V	N/A	0.4 V
In-series resistance	N/A	10 Ohm	N/A

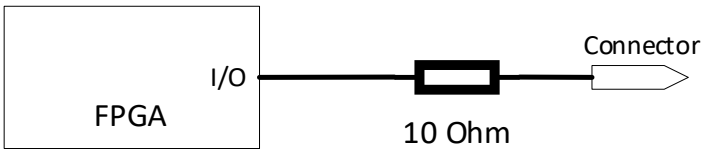

Figure 13: GPIO connection schematic

6.4 ADC interface

The ADC interface consists of 24 independent Delta-Sigma ADC converters. An additional ADC power interface is provided. The ADC interface is capable of measuring analogue values in the range from 0V to 3.3V.

Table 15: ADC interface electrical specifications

Parameter	Minimum	Typical	Maximum
Input voltage	0 V	N/A	3.3 V
Internal resistance*	N/A	100 kOhm	N/A
Power interface voltage	3.25 V	3.3 V	3.35 V
Power interface current	N/A	N/A	100 mA

* To internal VREF of 1.65 V

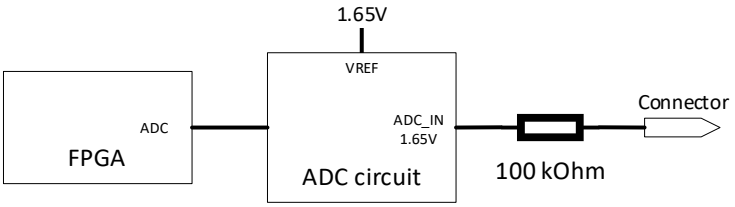

Figure 13: ADC connection schematic

6.5 FPGA JTAG Interface

JTAG interface is available on NANOif. The JTAG interface (P3) is used for flashing FPGA configuration. The JTAG interface is compliant to the standard 10-pin connector and can be used in conjunction with proprietary software provided by the FPGA manufacturer. The signal levels for the terminal interface are CMOS 3.3V.

NOTE: Do not use interface without SkyLabs approval, instruction and relevant equipment.

6.6 PicoSkyFT Processor Debug interface

The NANOif uses a dedicated Debug interface (P4) for accessing the embedded soft-core processor PicoSkyFT. Using a proprietary protocol and a PicoSky-Link programmer provides unified access to the internal registers of the processor, to all internal and external memories, and to all peripheral units of the NANOif. The signal levels of the PicoSky Debug interface are compliant with CMOS 3.3V levels. This interface is used for the firmware downloading to the NANOif's non-volatile memories. Furthermore, this interface provides unified debugging of the downloaded software using standard GNU (gcc, gdb) toolchain and propriety PicoSky-gdbproxy server.

NOTE: Do not use interface without SkyLabs approval, instruction and relevant equipment.

A. Appendix A

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