

nano-link-base-sb-2/nano-link-boost-sb-2/nano-linkboost-dp-sb-2

NANOlink Gen2 - Interface Control Document

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Approval of Document

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17/02/2021	1.11	Release	DSE	S 3	Updated power consumption figures.
				S 8	Clarified TX operation in regards to data in buffers.
30/03/2021	1.12	Release	DSE	S 3.2	Updated block diagram.
02/04/2021	1.13	Release	NFE	S 3.8	Updated centre of mass and added Mol.
09/04/2021	1.14	Release	DGA	S 2.3	Updated technical specifications - bandwidth.



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1 Introduction

1.1 Scope

The following document provides the Interface Control Document for the NANOlink 2nd generation, from hereinafter NANOlink.

1.2 Applicable Documents

Applicable Documents identified in the following text are identified by AD-n, where "n" indicates the actual document, from the following list:

AD#	Title	Doc. No.	Issue	Date
AD1	CAN-TS Protocol specifications		V1.4	12/06/2019
AD2	LVDS-TS Protocol specification		V1.1	12/03/2020
AD3	03 SkyLabs CCSDS Protocol V1.5 28/07/2		28/07/2020	
AD4	NANOlink Gen2 Software Interface Control Document		V1.10	30/03/2021

1.3 Reference Documents

Documents referenced in the following text, are identified by RD-n, where "n" indicates the actual document, from the following list:

RD#	Title	Doc. No.	Issue	Date
RD1	ROAD VEHICLES CONTROLLER AREA NETWORK (CAN) - PART 1: DATA LINK LAYER AND PHYSICAL SIGNALLING.	ISO Standard-11898-1		2013
RD2	PC/104-Plus Specification		Version 2.3	October 13, 2008

1.4 Acronyms and Abbreviations

AD	Applicable Documents
AR	Acceptance Review
BM	Breadboard Model
CCSDS	Consultative Committee for Space Data Systems
CDR	Critical Design Review
CLI	Command Line Interface
CoG	Centre of Gravity
COP	Communications Operations Procedure
CSP	Cost, Schedule, Performance
CTIA	Capacitive Trans Impedance Amplifier
DDJF	Design Development and Justification File
DDVP	Design Description and Verification Plan



EM EMC ESD	Engineering Model Electromagnetic Compatibility Electrostatic Discharge
FARM FOV	Frame Acceptance and Reporting Mechanism Field of view
FS	Feasibility study
FWHM	Full Width at Half Maximum
IC	Integrated Circuit
ICU	Interface and Control Unit
ICD	Interface Control Document
JTAG	Joint Test Action Group
LEO	Low Earth Orbit
NIY	Not Implemented Yet
NVM	Non-Volatile Memory
PDR	Preliminary Design Review
PFM	Proto Flight Model
PRR	Preliminary Requirements Review
RD	Reference Documents
OBC	On-Board Computer
QM	Qualification Model
QR	Qualification Review
SNR	Signal to Noise Ratio
SPU	SDR Processing Unit
SRR	System Requirements Review
TBC	To Be Confirmed
TBD	To Be Determined
ТВМ	Test Bench Model
TOA	Time of Arrival
UART	Universal Asynchronous Receiver/Transmitter
WBS	Work Breakdown Structure
WP	Work Package



2 NANOlink Overview

The NANOlink transceiver is designed for receiving and transmitting high data rates over large distances, while maintaining small size and mass and being the most power efficient product in its class. Highly miniaturised, NANOlink features in-orbit programmable SDR architecture, which enables the incorporation of various modulation schemes. High reliability is ensured via carefully selected parts and combined with an advanced FDIR approach that supervises the SDR logic and other critical parts of the subsystem. The full duplex communication subsystem is compliant with the SkyLabs CCSDS protocol, while supporting configurable modulation parameters and data rates. A highly efficient add-on RF amplifier module is available which boost the RF output power and together with NANOlink is called NANOlink-boost (nano-link-boost-sb-2). The architecture can be further expanded with the addition of a diplexer with integrated LNA, together forming the NANOlink-boost-dp (nano-link-boost-dp-sb-2). NANOlink features standard TM/TC channel via hot redundant CAN buses and a high speed LVDS interface.



Figure 1: NANOlink Gen2 (nano-link-base-sb-2) qualification model



Figure 2: NANOlink-boost Gen2 (nano-link-boost-sb-2) qualification model





Figure 3: NANOlink-boost-dp Gen2 (nano-link-boost-dp-sb-2) qualification model

2.1 Encoding and modulation overview

- Modulation
 - OQPSK modulation schemes
- Encoding
 - o CCSDS 231.0-B-3: TC Synchronization and Channel Coding
 - CCSDS 232.0-B-3: TC Space Data Link Protocol
 - CCSDS 131.0-B-3: TM Synchronization and Channel Coding
 - CCSDS 132.0-B-2: TM Space Data Link Protocol
 - o CCSDS 133.0-B-1 Cor.2: Space Packet Protocol
- Coding on TC:
 - BCH56
- Coding on TM:
 - Reed-Solomon 223, Convolution code ¹/₂
- Pulse shaping RRC filter (0.5 roll-off factor).
- 4 Mbps RX data rate with full, 1/2, 1/4, 1/8 data rate modes.
 - o 3.4 Mbps maximum TC user data due to CCSDS TC and BCH56 coding.
- 4 Mbps TX data rate with full, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64 data rate modes.
 - 1.6 Mbps maximum TM user data due to CCSDS TM, half-rate convolutional and Reed-Solomon coding.

2.2 Architecture overview

NANOlink hardware architecture is designed around an ICU, which is responsible for the management of the NANOlink. ICU interfaces directly with communication buses (e.g. CAN, SPI, TWI and UART), where it can be controlled to modify the SPU configuration, as well as read local telemetry data of the module or autonomously read telemetry data from other subsystems on the satellite. Primarily CAN interface is supported and presented in this document. Communication over other interfaces such as SPI, TWI and UART can be supported later upon customer request. The SPU is responsible for the configuration of the Transceiver, modulation and demodulation tasks as well as for CCSDS encoding/decoding (TM/TC data link and sync). It interfaces with the ICU via a raw bit-stream and it also supports a direct LVDS link to other on-board subsystems. The Transceiver is configured via a SPI bus, while the data transfer interface is a 12-bit parallel I-Q stream. The transceiver IC is responsible for transmitting the baseband I-Q stream and receiving the signal into the I-Q stream. It features dedicated up and down conversion circuits and integrated customizable FIR filters.



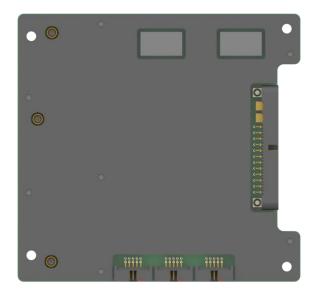


Figure 4: NANOlink-base - Top

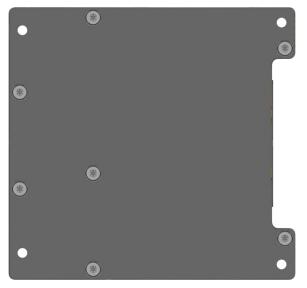


Figure 6: NANOlink-boost - Top



Figure 8: NANOlink-base - Side



Figure 10: NANOlink-boost - Front

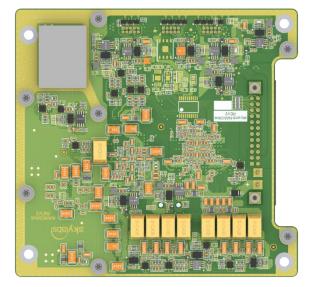


Figure 5: NANOlink-base - Bottom

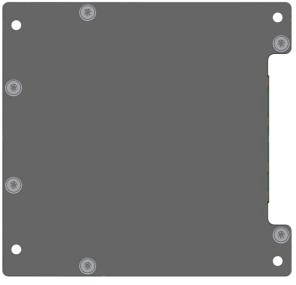


Figure 7: NANOlink-boost-dp - Top

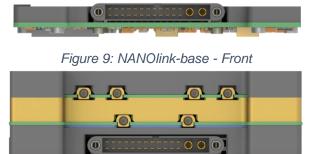


Figure 11: NANOlink-boost-dp - Front

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2.3 Technical specifications

Table 1: NANOlink Gen2 (nano-link-base-sb-2) - Technical specification

	Description	Comment
Output power	Adj. up to 30 dBm (1W)	
Output power dynamic range	60 dBm in 0.25 dB step	
Input sensitivity	-86 dBm @ 4 Mbps OQPSK	At 1E-3 BER TX enabled (at a different frequency), no preamp.
Supported modulations	OQPSK	other upon request
Noise figure	< 5 dB	
Data rates	default 4 Mbps @ 2.5 MHz (OQPSK)	downlink / uplink
Baseband bandwidth	up to 56 MHz	
Frequency band Transmitter Receiver	2.200 - 2.300 GHz 2.025 - 2.110 GHz	
On-board Communication interfaces	Redundant CAN bus for TM/TC LVDS for High-speed TM/TC data	Support for additional interfaces upon request (e.g. UART, SPI, I2C)
Supply voltage	5 V DC (+/- 10%)	For details please refer to section 3.3.
Power consumption	6 W (Rx + Tx @ 1W output power) 1.9 W (Rx only)	For details please refer to section 3.3.
Dimensions:	95 x 91 x 12 mm	For details please refer to section 3.8.
Operation temperature	-10°C to +50°C	For details please refer to section 3.9.1.
Storage temperature	-20°C to +65°C	For details please refer to section 3.9.1.
Mass:	110 g	For details please refer to section 3.8.

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Table 2: NANOlink-boost Gen2 (nano-link-boost-sb-2) - Technical specification

	Description	Comment
Output power	Adj. up to 37 dBm (5W)	
Output power dynamic range	60 dBm in 0.25 dB step	
Input sensitivity	-86 dBm @ 4 Mbps OQPSK	At 1E-3 BER TX enabled (at a different frequency), no preamp.
Supported modulations	OQPSK	other upon request
Noise figure	< 5 dB	
Data rates	default 4 Mbps @ 2.5 MHz (OQPSK)	downlink / uplink
Baseband bandwidth	up to 56 MHz	
Frequency band Transmitter Receiver	2.200 - 2.300 GHz 2.025 - 2.110 GHz	
On-board Communication interfaces	Redundant CAN bus for TM/TC LVDS for High-speed TM/TC data	Support for additional interfaces upon request (e.g. UART, SPI, I2C)
Supply voltage	5 V DC (+/- 10%)	For details please refer to section 3.3.
Power consumption	< 17 W (Rx + Tx @ 5W output power) < 1.9 W (Rx only)	For details please refer to section 3.3.
Dimensions:	95 x 91 x 22 mm	For details please refer to section 3.8.
Operation temperature	-10°C to +50°C	For details please refer to section 3.9.1.
Storage temperature	-20°C to +65°C	For details please refer to section 3.9.1.
Mass:	< 248 g	For details please refer to section 3.8.



Table 3: NANOlink-boost-dp Gen2 (nano-link-boost-dp-sb-2) - Technical specification

	Description	Comment
Output power	Adj. up to 32 dBm (1.5W) per antenna port.	Up to 2 dB losses on diplexer, joiner/splitter and additional filters.
Output power dynamic range	60 dBm in 0.25 dB step	
Input sensitivity	-86 dBm @ 4 Mbps OQPSK	At 1E-3 BER TX enabled (at a different frequency), no preamp.
Supported modulations	OQPSK	other upon request
Noise figure	< 5 dB	
Data rates	default 4 Mbps @ 2.5 MHz (OQPSK)	downlink / uplink
Baseband bandwidth	up to 56 MHz	
Frequency band Transmitter Receiver	2.200 - 2.300 GHz 2.025 - 2.110 GHz	
On-board Communication interfaces	Redundant CAN bus for TM/TC LVDS for High-speed TM/TC data	Support for additional interfaces upon request (e.g. UART, SPI, I2C)
Supply voltage	5 V DC (+/- 10%)	For details please refer to section 3.3.
Power consumption	< 17 W (Rx + Tx @ 5W output power from boost) < 1.9 W (Rx only)	For details please refer to section 3.3.
Dimensions:	95 x 91 x 32 mm	For details please refer to section 3.8.
Operation temperature	-10°C to +50°C	For details please refer to section 3.9.1.
Storage temperature	-20°C to +65°C	For details please refer to section 3.9.1.
Mass:	385 g	For details please refer to section 3.8.



3 Module specifications and generic parameters

3.1 Primary Function and Description

The NANOlink subsystem is a high-throughput CCSDS compliant communication module. It is built in a nanosatellite compatible PC-104 form factor, which consists of a primary board and an add-on RF amplifier module for the higher output power. In addition, NANOlink provides a communication channel for TM/TC via hot CAN-TS bus or high-speed LVDS interface.

NANOlink-base consists of the following building blocks:

- Adjustable SDR-based transceiver,
- An LNA on the RX path and a PA on the TX path with a power output of up to 30 dBm.
- Reprogrammable DSP-oriented FPGA for SDR functionality SDR processing unit,
- Robust FPGA for system control and monitor Interface and control unit,
- NVM memory storage (4 Mbytes).
- Dual CAN-TS bus.
- A High-speed point-to-point LVDS link (8b10b encoding) for high speed transmission.

With optional boost (NANOlink-boost):

• Additional power amplifier to boost power output to 37 dBm.

With optional diplexer (NANOlink-boost-dp):

- A splitter/combiner on two antenna ports,
- A diplexer connected to the splitter/combiner,
- An additional TX filter,
- An additional RX filter coupled with an LNA.

3.2 Module Block Diagram

The NANOlink subsystem is primarily centred around the use of Interface and control unit (ICU) and SDR processing unit (SPU) to provide a reconfigurable high-throughput communication system. The primary task of the ICU is to manage all the satellite-facing communication interfaces, which include the hot-redundant CAN bus supporting the CAN-TS. The ICU additionally supports the configuration of the SPU. It has access to an NVM memory, which is used to store SPU configuration.

The SPU in turn has control over the reconfigurable transceiver as also a direct high-speed communication interface to other subsystems via the 8b10b encoded LVDS. The transceiver is connected to an RX and TX RF chain. An additional output power monitor RF interface is also present. The transceiver further supports an RF calibration port.

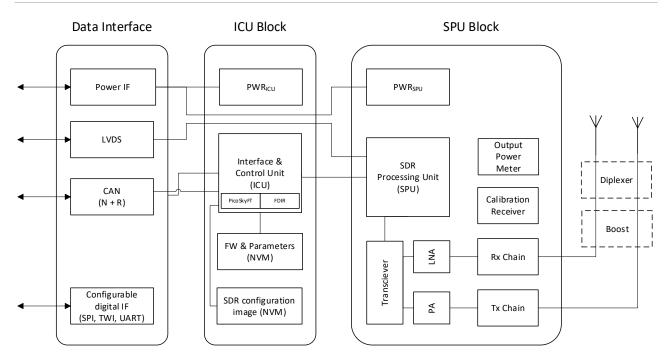


Figure 12: NANOlink-base Basic block diagram

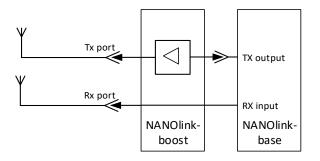


Figure 13: NANOlink-boost block diagram

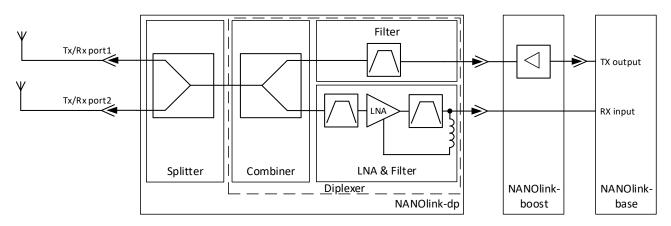


Figure 14: NANOlink-boost-dp block diagram

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3.3 Electrical Power

The NANOlink shall be powered with a 5V regulated power line. Other required voltages are generated internally with integrated DC-DC converters and linear regulators. Associated voltage ranges are 1.0 V, 1.2V, 1.3V, 1.8V, 2.5V, 3.3V and 5V.

Values are given for one NANOlink-base/NANOlink-boost/NANOlink-boost-dp.

Table 4: NANOlink-base Electri	ical characteristics
Num. of power interfaces:	1 (5 V, ±10%)
Voltages ranges:	1.0 V, 1.2 V, 1.3 V, 1.8 V, 2.5 V, 3.3 V, 5 V

Table 5: NANOlink-boost/NANOlink-boost-dp Electrical characteristics

Num. of power interfaces:	1 (5 V, ±10%)
Voltages ranges:	-3.0 V, 1.0 V, 1.2 V, 1.3V, 1.8 V, 2.5 V, 3.3 V, 5 V, 28 V

Table 6: NANOlink-base Power consumption

Power consumption	At 25 °C	At -35 °C	At 70 °C
RX only mode • All CAN channels terminated.	1.62 W	1.58 W	1.82 W
 TX on mode All CAN channels terminated. 30 dBm output power 	6.0 W	5.8 W	6.2 W
IDLE mode All CAN channels terminated. 	0.56 W	0.57 W	0.61 W

Table 7: NANOlink-boost/boost-dp Power consumption

Power consumption	At 25 °C	At -35 °C	At 70 °C
RX only mode All CAN channels terminated. 	1.63 W	1.59 W	1.83 W
 TX on mode All CAN channels terminated. 37 dBm output power (boost) 32 dBm output power per channel (boost-dp) 	Less than 17 W	Less than 17 W	Less than 17 W
IDLE mode • All CAN channels terminated.	0.57 W	0.58 W	0.62 W

3.3.1 Inrush current profile

The inrush current of the NANOlink is defined by the input capacitances of the NANOlink local power supply DC-DC converters. There is no active inrush limiting circuitry present on the NANOlink.

Table 8: NANOlink-base/NANOlink-boost/NANOlink-boost-dp Inrush current characteristics

Equivalent input capacitance	140 uF	
Inrush profile (lead connected to 5V power supply, no soft start):		
Inrush duration	40 us	



• Inrush peak	25 A
Inrush charge transferred (0V to 5V)	0.65 mAs

3.3.2 Turn off/on procedure

The on/off procedure of NANOlink is to switch on/off its power supply line. NANOlink is insensitive to hard resets.

3.4 Grounding Scheme

The whole NANOlink uses a single common ground topology. All parts of the NANOlink share a common ground. All mechanical parts of the NANOlink are grounded. All RF cable shields are grounded. All connector pins with the signal type marked as GND refer to this common ground potential. Additional ground signal types are:

- CAN ground: connected to GND through a 0 Ohm resistor near the CAN driver.
- LVDS shield: connected to GND through a 0 Ohm resistor near the LVDS driver.

3.5 Electro Static Discharge

The NANOlink contains sensitive electronic components that are susceptible to be damaged by static electricity. When handling or installing the NANOlink observe appropriate precautions and ESD safe practices.

3.6 Electromagnetic Compatibility

Each NANOlink can be upon request RF characterised and tested for EMC, according to ECSS-E-ST-20-07C. Tests are performed in facility certified for CCA EMC test procedures.

3.7 Mechanical Interface Control Drawing

The NANOlink is fully compliant to PC104 mounting specifications. For standard details please refer to RD2. NANOlink electronics board is fixed into common PC/104 compliant fixation rod. Cable stripes are used to provide power and establish communication link between NANOlink and other command and data handling equipment, over CAN and high speed LVDS interfaces.

Please take special care when designing mechanical stack up, to keep clear of exposed components of the NANOlink subsystem on the bottom side. It is recommended to provide a clearance between this and another component in stack up of at least 2 mm on the and bottom side.



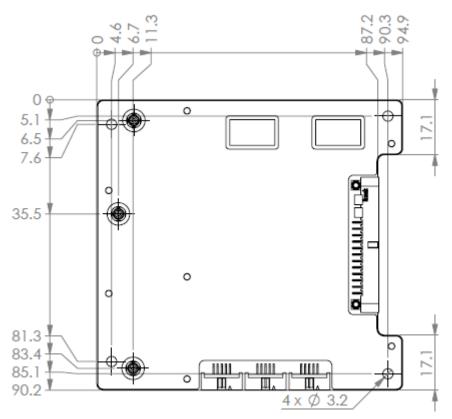


Figure 15: Mechanical Drawing of NANOlink-base - Top view

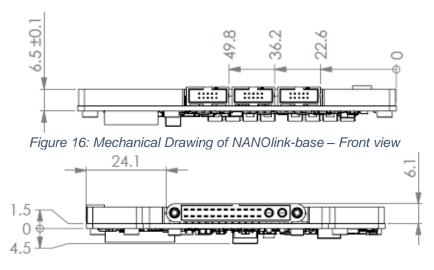
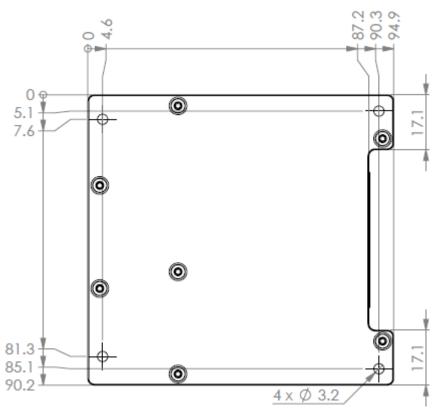


Figure 17: Mechanical Drawing of NANOlink-base - Side view

Non-confidential







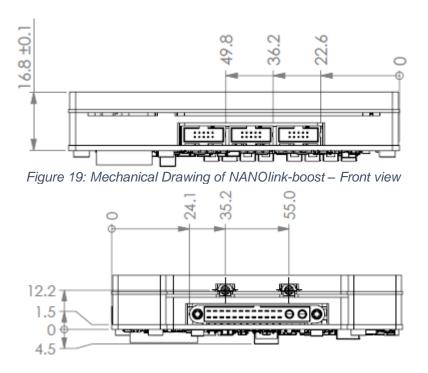


Figure 20: Mechanical Drawing of NANOlink-boost - Side view



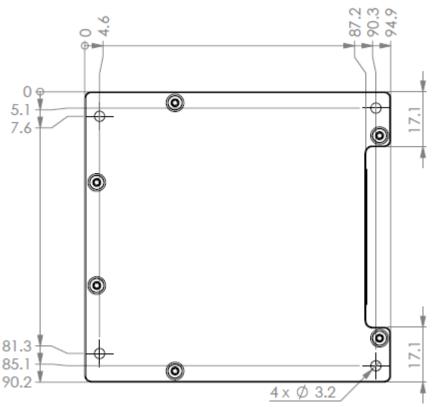


Figure 21: Mechanical Drawing of NANOlink-boost-dp - Top view

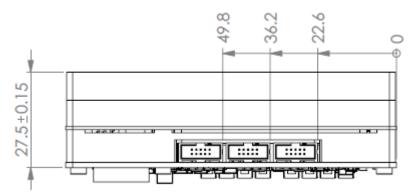


Figure 22: Mechanical Drawing of NANOlink-boost-dp - Front view

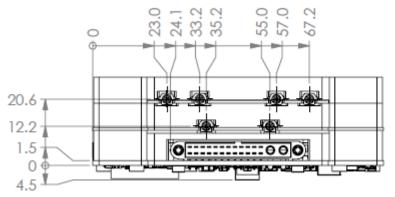
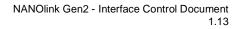


Figure 23: Mechanical Drawing of NANOlink-boost-dp – Side view

Non-confidential





3.8 Mechanical Interface Control parameters

NANOlink Gen2 mechanical properties:

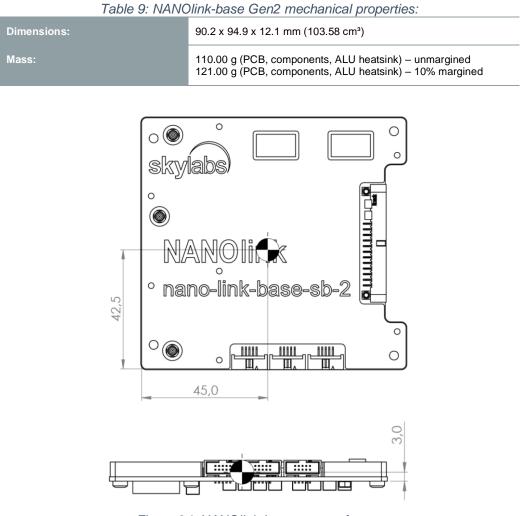


Figure 24: NANOlink-base centre of mass

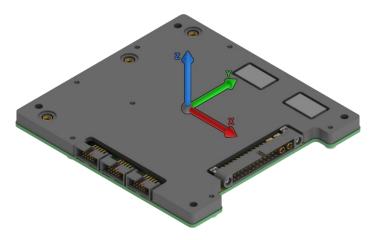


Figure 25: NANOlink-base reference coordinate system

Moments of inertia: (grams * square millimeters)

Taken at the centre of mass (Figure 24) and aligned with the output coordinate system (Figure 25).

Table 10: NANOlink-base moments of Inertia



Lxx = 90915.27	Lxy = 790.89	Lxz = 238.69
Lyx = 790.89	Lyy = 78429.55	Lyz = -241.14
Lzx = 238.69	Lzy = -241.14	Lzz = 168157.61

NANOlink-boost Gen2 mechanical properties:

Table 11: NANOlink-boost Gen2 mechanical properties:	
Dimensions:	90.2 x 94.9 x 21.3 mm (182.33 cm³)
Mass:	225.00 g (PCB, components, ALU heatsink) – unmargined 248.00 g (PCB, components, ALU heatsink) – 10% margined

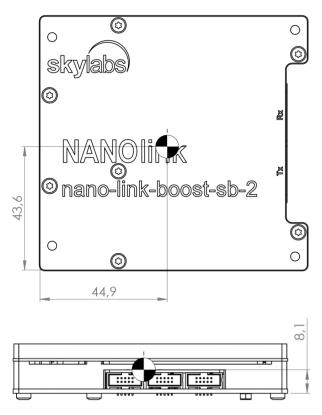


Figure 26: NANOlink-boost centre of mass



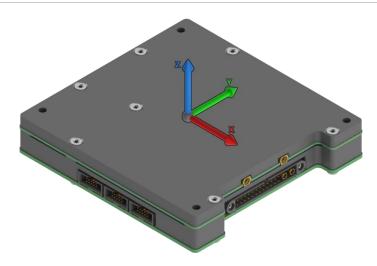


Figure 27: NANOlink-boost reference coordinate system

Moments of inertia: (grams * square millimeters)

Taken at the centre of mass (Figure 26) and aligned with the output coordinate system (Figure 27).

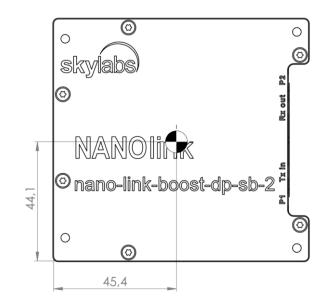
Lxx = 184945.58	Lxy = 193.82	Lxz = -272.65
Lyx = 193.82	Lyy = 172853.75	Lyz = 548.00
Lzx = -272.65	Lzy = 548.00	Lzz= 346504.53

Table 12: NANOlink-boost moments of Inertia

NANOlink-boost-dp Gen2 mechanical properties:

Table 13: NANOlink-boost-dp Gen2 mechanical properties:

Dimensions:	90.2 x 94.9 x 32.0 mm (273.91 cm³)
Mass:	385.00 g (PCB, components, ALU heatsink) – unmargined 405.00 g (PCB, components, ALU heatsink) – 5% margined





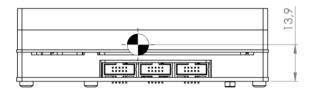


Figure 28: NANOlink-boost-dp centre of mass

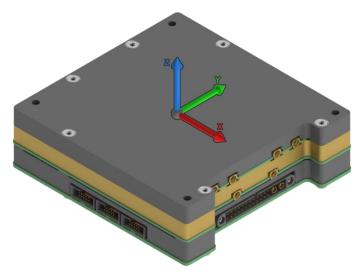


Figure 29: NANOlink-boost-dp reference coordinate system

Moments of inertia: (grams * square millimeters)

Taken at the centre of mass (Figure 28) and aligned with the output coordinate system (Figure 29).

Table 14. NANOIIOIR-boost-up moments of menta			
Lxx = 325427.93	Lxy = -144.85	Lxz = 703.30	
Lyx = -144.85	Lyy = 319742.89	Lyz = 2090.28	
Lzx = 703.30	Lzy = 2090.28	Lzz = 594457.06	

Table 14: NANOlionk-boost-dp moments of Inertia

3.8.1 Materials specifications

Material	Manufacturer	%TML	%CVCM	%WVR	Application	Note
Aluminium 6082-T6 Anodized and dyed black	Riedl			/	Shield	All shields except for single shield in NANOlink-boost-dp
Aluminium 6082-T6 Galvanized then electroplated with copper (Cu) and 1 um of gold (Au)	Riedl			1	Shield	NANOlink-boost-dp middle shield
PCB material for Base	ISOLA 370HR			0.15	PCB board	ECSS identified
PCB material for Boost and Diplexer	RO4003				PCB board	
Solder	SAC305				Soldering	



Thermal interface material GAP	Bergquist	0.21	0.08	Thermal
PAD HC 3.0				Interface

3.8.2 List and location of thermal sensors

Sensor	Name	Туре	PCB location
T1	ICU FPGA Sensor	External NTC (B=3380)	Bottom
T2	SPU FPGA Sensor	Internal Sensor of FPGA	Тор
Т3	Regulator Sensor	Internal Sensor of Power Regulator	Тор
T4	Regulator Sensor	Internal Sensor of Power Regulator	Тор
T5	PA Sensor	External NTC (B=3380)	Bottom
Т6	PDET Sensor	Internal Sensor of IC	Bottom
Τ7	Boost PA Sensor	External NTC (B=3380) Top	

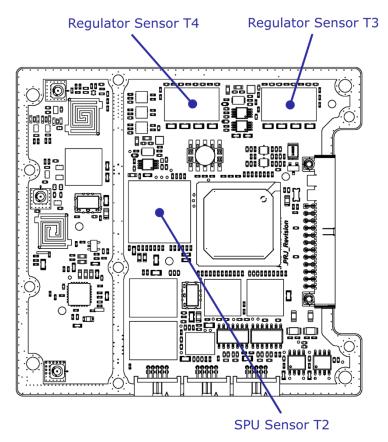


Figure 30: Location of NANOlink-base Thermal Sensors – Base board Top



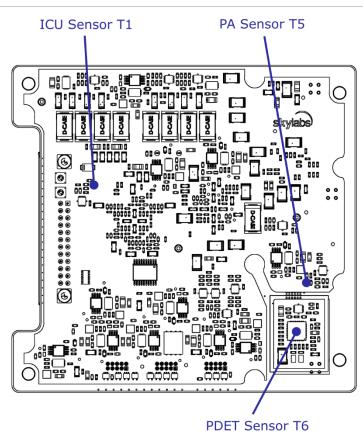


Figure 31: Location of NANOlink-base Thermal Sensors - Base board Bottom

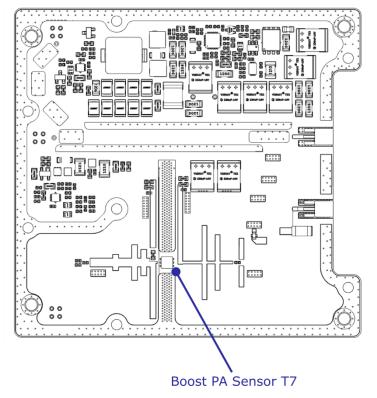


Figure 32: Location of NANOlink-boost Thermal Sensors -Boost board Top

Module specifications and generic parameters Copyright © 2021 SkyLabs. All rights reserved.



3.9 Environmental Requirements

3.9.1 Thermal Limits

Table below describes the thermal limits for the NANOlink. Recommended values for all electronic modules are provided in the table.

The definition of the Design, Acceptance and Qualification limits are as follows:

- **Design Temperature**: The temperature to which the flight equipment can operate in service and work satisfactorily.
- **Qualification Temperature**: The temperature to which the module design has been tested and proven to work satisfactorily.
- Acceptance Temperature: The temperature to which the flight equipment has been tested and proven to work satisfactorily.

	Design	Qualification	Acceptance
Non-operating temperature limits	-35°C - +75°C	-30°C - +70°C	-25°C - +65°C
Start-up temperature limits	-20°C - +60°C	-15°C - +55°C	-10°C - +50°C
Operating temperature limits	-30°C - +60°C	-25°C - +55°C	-20°C - +50°C

3.9.2 Thermal Dissipation

This section provides information on the thermal dissipation of the NANOlink modules, in Watts.

Thermal dissipation will be less than estimated power consumption for each module.

Table 16: NANOlink Power Dissipation

	Power Dissipation [W]	Primary thermal path
NANOlink-base	< 5 W	To PCB fixation holes, also through Alu shield.
NANOlink-boost	< 10 W	To PCB fixation holes, also through Alu shield.
NANOlink-boost-dp	< 10 W	To PCB fixation holes, also through Alu shield.

3.9.3 Definition of External Surface Properties

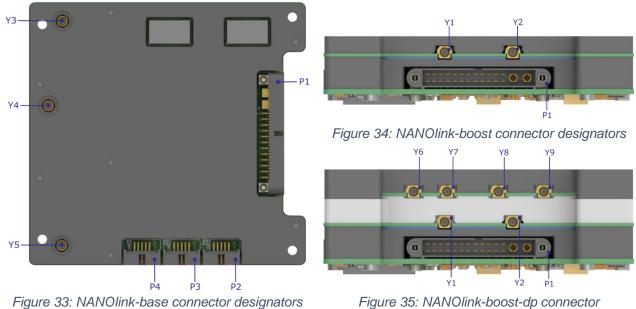
NANOlink and NANOlink-boost shields are black anodised. The middle NANOlink-boost-dp shield is galvanized then electroplated with copper (Cu) and 20 um of silver (Ag).



4 Harness

NANOlink provides power and communication interface connector in the same package.

4.1 NANOlink Connectors



designators

4.1.1 NANOlink-base Power and Signal Connector

Connector name:	NANOlink-base Power and Communication connector
Connector designator:	P1
Connector function:	Power supply and communication interface
Connector type:	Multi-mix connector, power and signal to the Board, MALE
Connector part number:	221V24F26-0200-3400CMM
Mate connector part number:	222S24M16-0200-4310

23 21 19 17 15 13 11 9 7 5 3 1 24 22 20 18 16 14 12 10 8 6 4 2 B A

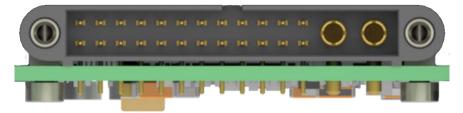


Figure 13: NANOlink-base Power and Signal Connector (221V24F26-0200-3400CMM)



Table 17: NANOlink-base Power and Signal connector pins (221V24F26-0200-3400CMM)

Pin	Signal Name	Signal Type	Wire Type	Notes
A	Power +5V	+5 V power supply	AWG-16	
В	Power GND	GND	AWG-16	
1	CANB_P	CAN signal level	AWG-26	Redundant bus
2	CANB_N	CAN signal level	AWG-26	Redundant bus
3	CANB GND	CAN ground	AWG-26	Redundant bus
4	CANA GND	CAN ground	AWG-26	Nominal bus
5	CANA_P	CAN signal level	AWG-26	Nominal bus
6	CANA_N	CAN signal level	AWG-26	Nominal bus
7	LVDS1_SHD	LVDS TX cable shield	AWG-26	
8	LVDS0_TX_P	LVDS signal level	AWG-26	
9	LVDS1_TX_P	LVDS signal level	AWG-26	
10	LVDS0_TX_N	LVDS signal level	AWG-26	
11	LVDS1_TX_N	LVDS signal level	AWG-26	
12	LVDS0_RX_N	LVDS signal level	AWG-26	
13	LVDS1_RX_N	LVDS signal level	AWG-26	
14	LVDS0_RX_P	LVDS signal level	AWG-26	
15	LVDS1_RX_P	LVDS signal level	AWG-26	
16	LVDS0_SHD	LVDS TX cable shield	AWG-26	
17	GPIO7	GPIO	AWG-26	GPIO0_7
18	GPIO6	GPIO	AWG-26	GPIO0_6
19	GPIO5	GPIO	AWG-26	GPIO0_5
20	GPIO4	GPIO	AWG-26	GPIO0_4
21	GPIO3	GPIO	AWG-26	GPIO0_3
22	GPIO2	GPIO	AWG-26	GPIO0_2
23	GPIO1	GPIO	AWG-26	GPIO0_1
24	GPIO0	GPIO	AWG-26	GPIO0_0

4.1.2 NANOlink-base RF Connectors

Connector name:

NANOlink RF connectors (Multiple, check tables below)



Connector function:RFConnector type:50 Ohms, SMPM Plug, PCB Mount, VerticalConnector part number:73300-0080

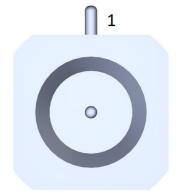


Figure 36: NANOlink RF Connector (73300-0080)

4.1.2.1 Receive Connector name:	Signal Conn		e RF Receive signal	
Connector designa	tor:	Y3		
Table 18: NA		ANOlink RF Recei	ive signal connector pin (73300	0-0080) (F3)
	Pin	Signal Name	Signal Type	Notes
-	1	RF_RX_IN	Receive signal input (with LNA + bandpass filter)	
4.1.2.2 Calibratio	on Receive S	Signal Connector		
Connector name:		NANOlink-base	e RF Calibration receive sign	al
Connector designa	tor:	Y4		
Table	19: NANOI	ink RF Calibration Signal Name	receive signal connector pin (Signal Type	73300-0080) (F4) Notes
		RF_RX_CAL_IN	Receive signal input without LNA (for calibration)	
4.1.2.3 Transmit	Signal Con	nector		
Connector name:		NANOlink-base	e RF Transmit signal	
Connector designa	tor:	Y5		
	Table 20: NA	ANOlink RF Trans	mit signal connector pin (7330	0-0080) (F5)
I	Pin	Signal Name	Signal Type	Notes
	1	RF_TX_PA_OUT	Transmit signal output	
413 NANOlin	k-boost R	F Connector		

4.1.3 NANOlink-boost RF Connector

Connector name:	NANOlink-boost RF connectors (check table below)
Connector function:	RF



Connector type:

50 Ohms, SMPM Plug, PCB Mount, Straight

Connector part number: 925-126J-51P

In case of NANOlink-boost option, the RF connectors Y6, Y7, Y8 and Y9 on NANOlink are unavailable for user. For transmitter output signal on NANOlink-boost Y1 RF connector shall be used. The NANOlink Y2 connector for RF received signal is used in case of the NANOlink-boost configuration instead of Y3.

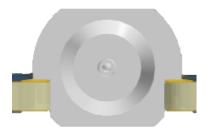


Figure 37: NANOlink-boost RF Connector (925-126J-51P)

4.1.3.1 Transmit Signal Connector

Connector name:

NANOlink-boost RF Transmit signal

Y1

Connector designator:

Table 21: NANOlink-boost RF Transmit signal connector pin (925-126J-51P) (Y1)

Pin	Signal Name	Signal Type	Notes
1	RF_TX_BOOST_OUT	Transmit signal output	

4.1.3.2 Receive Signal Connector

Connector name: NANOlink-boost RF Receive signal

Y2

Connector designator:

 Table 22: NANOlink-boost RF Receive signal connector pin (925-126J-51P) (Y2)

 Pin
 Signal Name
 Signal Type
 Notes

 1
 RF_RX_BOOST_IN
 Receive signal input

4.1.4 NANOlink-boost-dp RF Connector

Connector name:	NANOlink-boost-dp RF connectors (check table below)
Connector function:	RF
Connector type:	50 Ohms, SMPM Plug, PCB Mount, Straight
Connector part number:	925-126J-51P

In case of NANOlink-boost-dp option, the RF connectors Y1 and Y2 on the NANOlink-boost are unavailable for use. Instead, the NANOlink-boost-dp is provided with the connectors Y1 and Y2 connected with Y7 and Y8 respectively through a provided RF cable. For transmitted output signal and received input signal on NANOlink-boost-dp Y6 and Y9 connectors shall be used.



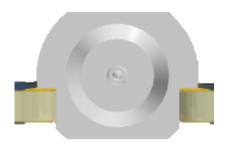


Figure 38: NANOlink-boost RF Connector (925-126J-51P)

<i>4.1.4.1 Transmit Signal</i> Connector name:		st-dp RF RX/TX port 1	
Connector designator:	Y6		
Table 23: NA	ANOlink-boost RF Tran	smit signal connector pin (92	25-126J-51P) (
Pin	Signal Name	Signal Type	Notes
1	RF_RXTX1_BOOST	Transmit signal input/output	
4.1.4.2 Transmit Signal	Input Connector		
Connector name:		st-dp RF Transmit Input sig	Inal
Connector designator:	Y7		
Table 2 <u>4: NAN</u>	Olink-boost RF Transm	nit Input signal connector pin	(925-126J-51)
Pin	Signal Name	Signal Type	Notes
		olgilai i jpo	
1	RF_TX_BOOST_IN	Transmit signal input	
1 4.1.4.3 Receive Signal (Connector name:	RF_TX_BOOST_IN Dutput Connector NANOlink-boos		gnal
1 4.1.4.3 Receive Signal (Connector name: Connector designator:	RF_TX_BOOST_IN Dutput Connector NANOlink-boos Y8	Transmit signal input	-
1 4.1.4.3 Receive Signal (Connector name: Connector designator:	RF_TX_BOOST_IN Dutput Connector NANOlink-boos Y8	Transmit signal input	-
1 4.1.4.3 Receive Signal (Connector name: Connector designator: Table 25: NANC	RF_TX_BOOST_IN Dutput Connector NANOlink-boos Y8 Dlink-boost RF Receive	Transmit signal input	n (925-126J-51
1 4.1.4.3 Receive Signal (Connector name: Connector designator: Table 25: NANC Pin	RF_TX_BOOST_IN Dutput Connector NANOlink-boos Y8 Dlink-boost RF Receive Signal Name RF_RX_BOOST_OUT Connector	Transmit signal input	n (925-126J-51
1 4.1.4.3 Receive Signal (Connector name: Connector designator: Table 25: NANC Pin 1 4.1.4.4 Receive Signal (Connector Signal (Connector designator))	RF_TX_BOOST_IN Dutput Connector NANOlink-boos Y8 Dlink-boost RF Receive Signal Name RF_RX_BOOST_OUT Connector	Transmit signal input st-dp RF Receive Output signal o <i>Output signal connector pin</i> Signal Type Receive signal output	n (925-126J-51
14.1.4.3Receive Signal (Connector name:Connector designator:Table 25: NANCPin14.1.4.4Receive Signal (Connector name:Connector designator:Connector designator:	RF_TX_BOOST_IN Dutput Connector NANOlink-boos Y8 Dlink-boost RF Receive Signal Name RF_RX_BOOST_OUT Connector NANOlink-boos Y9	Transmit signal input st-dp RF Receive Output signal o <i>Output signal connector pin</i> Signal Type Receive signal output	9 (925-126J-51 Notes
14.1.4.3Receive Signal (Connector name:Connector designator:Table 25: NANCPin14.1.4.4Receive Signal (Connector name:Connector designator:Connector designator:	RF_TX_BOOST_IN Dutput Connector NANOlink-boos Y8 Dlink-boost RF Receive Signal Name RF_RX_BOOST_OUT Connector NANOlink-boos Y9	Transmit signal input st-dp RF Receive Output signal o Output signal connector pint Signal Type Receive signal output	9 (925-126J-51 Notes



5 Telecommands and Telemetry

The primary access mechanism for the telecommands and the telemetry of the NANOlink subsystem is through the CAN interface. Alternatively, it is possible to access the same telecommands and telemetry via the RF link.

The details of the telecommands and telemetry can be found in [AD4].

5.1 NANOlink TC&TM access: CAN interface

The CAN interface of the NANOlink subsystem is fully compatible with the CAN-TS protocol. Refer to the CAN-TS documentation [AD1] for more details.

5.2 NANOlink TC&TM access: RF link

As an alternative to TC&TM access over the CAN interface, it is possible to perform equivalent accesses over the RF interface. Refer to the SkyLabs CCSDS specification [AD3] for more details.

5.3 LVDS commands

The interface over the LVDS link is fully compatible with the LVDS-TS protocol [AD2]. The interface defines no commands, as it is only accessible over the RF link and such always managed via the RF interface.



6 Operations

The details of the operations as well as a full description of the operating modes can be found in [AD4].



7 Interfaces - Electrical Characteristics

7.1 CAN interface

Controller–area network (CAN or CAN-bus) is an automotive bus standard designed to allow microcontrollers and devices to communicate with each other within a vehicle without a host computer. CAN is a message-based protocol, designed specifically for automotive applications but is now also used in other areas, such as industrial automation, medical equipment, and for space applications.

CAN is a multi-master broadcast serial bus standard for connecting Electronic Control Units (ECUs). Each node is able to send and receive messages, but not simultaneously. A message consists primarily of an id, which represents the priority of the message, and up to eight data bytes. It is transmitted serially onto the bus. This signal pattern is encoded in Non-Return-to-Zero (NRZ) and is sensed by all nodes.

The devices that are connected by a CAN network are typically sensors, actuators, and other control devices. These devices are not connected directly to the bus, but through a host processor and a CAN controller.

If the bus is free, any node may begin to transmit. If two or more nodes begin sending messages at the same time, the message with the more dominant ID (which has more dominant bits, i.e., zeroes) will overwrite other nodes' less dominant ID's, so that eventually (after this arbitration on the ID) only the dominant message remains and is received by all nodes. This mechanism is referred to as priority-based bus arbitration. Messages with numerically smaller values of ID have higher priority and are transmitted first.

NANOlink TM/TC is based on CAN Specification [RD1], Version 2 Bosch GmbH – CAN standard B, 29-bit Identifier, at the application layer the CAN-TS protocol, developed SkyLabs is used for all communications in and out of NANOlink subsystem.

The CAN standard requires that the CAN bus is terminated at each end by a one-hundred-and-twenty-ohm resistor. It is possible that the termination resistors are fitted in the harness/connector and not in the module.

7.1.1 CAN Physical Interface

7.1.1.1 CAN Physical Interface electrical specifications

Table 27: CAN Interface electrical specifications

Parameter	Minimum	Typical	Maximum
Maximum DC voltage	-58V	N/A	58V
Maximum transient voltage	-150V	N/A	100V
Maximum current	-40mA	N/A	100mA
ESD discharge (HBM) *	- 8kV	N/A	+8kV
ESD discharge (IEC 61000-4-2) *	- 8kV	N/A	+8kV

* Discharge at available pins CANH and CANL on connector

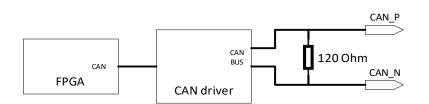


Figure 13: CAN interface schematic (note: 120 Ohm termination resistor optional)



7.1.2 CAN Redundancy Operation

NANOlink support communication over cold or hot redundant CAN busses. In case hot redundant networking topology is not considered in satellite, hot redundant operation can be disabled.

Hot redundant operation means that transmitting CAN node transmits single frame throughout both CAN busses concurrently. Receiving CAN nodes are listening on both CAN busses, where receiving CAN arbiter selects bus, on which the CAN frame arrived first. In case of detecting concurrent reception, arbiter always select primary CAN bus (CAN_A).

7.2 LVDS Interface

The LVDS interface can provide data rates up to 20Mbps while bus-terminal ESD exceeds 12 kV and operates in wide temperature range. Selected LVDS physical driver is intended for use in simplex or distributed simplex bus structures, the driver enable function does not put the differential outputs into a high-impedance state, but rather disconnects the input and reduces the quiescent power used by the device. Differential driver and receiver meet or exceed the requirements of the ANSI TIA/EIA-644-1995 standard.

7.2.1.1 LVDS electrical specifications

Parameter	Minimum	Typical	Maximum
Differential output voltage	247 mV	340 mV	454 mV
Change between differential output voltage	-50 mV	NA	50 mV
Steady-state common-mode output voltage	1.125 V	1.2 V	1.375 V
Peak to peak common-mode output voltage	NA	50 mV	150 mV

Table 29: LVDS receiver electrical specifications

Parameter	Minimum	Typical	Maximum
Positive-going differential input voltage threshold	NA	NA	100 mV
Negative-going differential input voltage threshold	-100 mV	NA	NA
High level output voltage	2.4-2.8 V	NA	NA
Low level output voltage	0.4 V	NA	NA

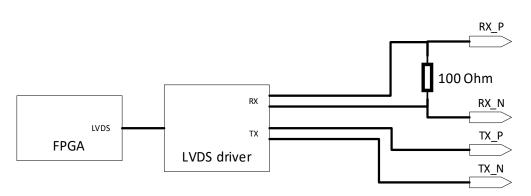
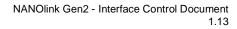


Figure 13: LVDS interface schematic





7.3 GPIO Interface

The GPIO interfaces feature general purpose I/Os with I/O remapping capability (capability to use GPIO pins for alternative functions, such as PWM, UART, I2C, SPI, etc.). The GPIO interface follows the LVCMOS 3.3V standard.

All GPIO pins are connected to FPGA I/O pins, with a 10 Ohm resistor in series.

Parameter	Minimum	Typical	Maximum
Input current	N/A	N/A	10 uA
DC Input High	2.0 V	N/A	3.45 V
DC Input Low	-0.3 V	N/A	0.8 V
Output current	N/A	N/A	12 mA
DC Output High	2.9 V	N/A	3.3 V
DC Output Low	0.0 V	N/A	0.4 V
In-series resistance	N/A	10 Ohm	N/A

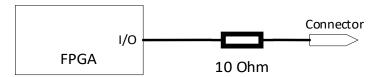


Figure 13: GPIO connection schematic

7.4 ICU FPGA JTAG Interface – P3

JTAG interface is available on NANOlink. The JTAG interface (connector designator: P3) is used for flashing ICU FPGA configuration. The JTAG interface is compliant to the standard 10-pin connector and can be used in conjunction with proprietary software provided by the FPGA manufacturer. The signal levels for the terminal interface are CMOS 3.3V.

NOTE: Do not use interface without SkyLabs approval, instruction and relevant equipment.

7.5 SPU FPGA JTAG Interface – P4

JTAG interface is available on NANOlink. The JTAG interface (connector designator: P4) is used for uploading SPU FPGA configuration. The JTAG interface is compliant to the standard 10-pin connector and can be used in conjunction with proprietary software provided by the FPGA manufacturer. The signal levels for the terminal interface are CMOS 3.3V.

NOTE: Do not use interface without SkyLabs approval, instruction and relevant equipment.

7.6 PicoSkyFT Processor Debug interface – P2

The NANOlink uses a dedicated Debug interface (connector designator: P2) for accessing the embedded softcore processor PicoSkyFT. Using a proprietary protocol and an PicoSky-Link programmer provides unified access to the internal registers of the processor, to all internal and external memories, and to all peripheral units of the NANOlink. The signal levels of the PicoSky Debug interface are compliant with CMOS 3.3V levels. This interface is used for the firmware downloading to the NANOlink's non-volatile memories. Furthermore, this interface provides unified debugging of the downloaded software using standard GNU (gcc, gdb) toolchain and propriety PicoSky-gdbproxy server.

NOTE: Do not use interface without SkyLabs approval, instruction and relevant equipment.



8 Space-Ground Communication

All space-ground is handled via the RF link over a CCSDS compliant interface. The protocol used is the SkyLabs CCSDS protocol [AD3].

The NANOlink subsystem supports the following VCNs:

- CAN VCN: Single CAN transfer
- MASS VCN: Burst CAN transfer
- Beacon VCN: Beacon function
- Ranging VCN: Ranging function
- LVDS VCN: LVDS transfer

8.1 Message handling between CCSDS protocol and On-board Interfaces

8.1.1 CAN VCN

As such, it is possible for a CAN message to be handled locally by the NANOlink subsystem, without any access to the CAN interface. All CAN messages originating from the CCSDS stream are sent over the Comm address of the NANOlink. The following scenarios are envisioned:

- NANOlink receives a non-local CAN message from the CCSDS stream. It sends this message via the CAN interface and waits for a reply. If a timeout occurs without receiving the response, the CAN message is resent up to a configurable number of times. If a response is never received, the message is silently dropped. When a response is received, it is forwarded via the CCSDS stream.
- NANOlink receives a local CAN messages. It handles it locally and the reply is forwarded via the CCSDS stream.
- NANOlink receives a CAN message from the CAN interface addressed to the Comm address. It sends
 a response (if applicable) to the message over the CAN interface and forwards the message via the
 CCSDS stream.

8.1.2 MASS VCN

Mass transfers are handled by the ICU unit. As such, it is possible for a Mass transfer to be handled locally by the NANOlink subsystem, without any access to the CAN interface. All Mass transfers originating from the CCSDS stream are sent over the Comm address of the NANOlink. The following scenarios are envisioned:

- NANOlink receives a non-local Mass transfer message from the CCSDS stream. It then performs the Mass transfer via the CAN interface according to the CAN-TS protocol. If a timeout occurs during any message, the whole transfer is aborted and repeated up to a configurable number of times. After the whole transfer is successfully completed, the response is forwarded via the CCSDS stream. If the transfer is not successfully completed, it is silently dropped. If a NACK is received to the request message of the Mass transfer, a NACK response is forwarded via the CCSDS stream.
- NANOlink receives a local Mass transfer. It handles it locally and the reply is forwarded via the CCSDS stream.

Mass transfers via the CCSDS protocol are only supported when the NANOlink is the originating system of the transfers. Mass transfer requests sent to the Comm address of the NANOlink will be rejected with a NACK.

8.1.3 BEACON VCN

The function of the beacon is to provide a periodic unsolicited RF stream that allows basic troubleshooting of the satellite in case of any problems. It functions as a periodic (configurable period) CCSDS stream, that contains keep-alive messages received by the NANOlink subsystem. The following scenario is envisioned:

• NANOlink received a Keep-alive message. It stores the message locally, and then when the once per Beacon period, it forwards all the stored Keep-alive messages via the CCSDS stream.



8.1.4 LVDS VCN

LVDS messages are handled directly be the SPU unit. As such, they cannot be used to communicate with the NANOlink subsystem. The following scenarios are envisioned:

- NANOlink receives a LVDS message from the CCSDS stream. It sends this message over the LVDS interface. It then waits for a response. If a timeout occurs without receiving the response, the LVDS message is resent up to a configurable number of times. If a response is never received, the message is silently dropped. When a response is received, it is forwarded via the CCSDS stream.
- NANOlink receives a LVDS message from the LVDS interface. It sends a response over the LVDS interface and forwards the received LVDS message via the CCSDS stream.

8.2 Transmission behaviour

The transmission behaviour of the NANOlink unit is highly configurable. As such, this section gives an overview of the transmitting behaviour of the NANOlink in various modes.

In general, two modes can be selected that affect the NANOlink transmitting behaviour: "RX on, TX on" and "RX on, TX automatic". The difference between the modes in that in "TX on" mode, the transmitter is enabled when the system enters this mode and is not turned off until the operating mode is changed, or if an error occurs. In contrast, if the system is in "TX automatic", the transmitter is only enabled when data was scheduled to be sent. The transmitter then automatically turns off when all the data was transmitted.

In both modes, there are two possibilities on what is being transmitted. If there is not data to be sent, then a PRNG sequence is continuously transmitted. The PRNG sequence is a raw PRNG bitstream – no encoding is used when it is being sent. If there is data to be sent, valid TM frames are sent. The system considers the following scenarios as "data available to send":

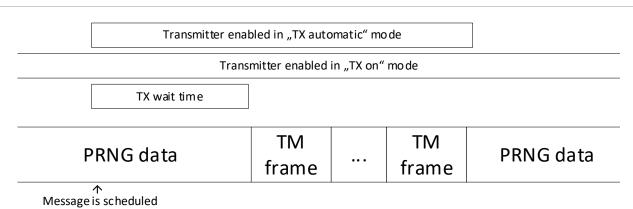
- The user performed an action that generates data to be sent. For example:
 - A CAN or MASS message or acknowledgement with the Comm destination address is received.
 - A LVDS message is received.
 - A SPP over CAN or SPP over LVDS message is received.
 - A beacon message is scheduled in "TX on" mode.
 - \circ The beacon period expires in "TX automatic" mode.
 - A TC message is received that requires a response over the COP-1 mechanism.

When any of the above actions occur, the data is sent in the order compliant with the one specified in the VC multiplexing scheme in [AD3]. TM messages are transmitted until there is data available to transmit. If additional data is generated while transmission is in progress, the data is sent in the next TM frames. When no more data is available to send the system reverts to sending PRNG data and continues to do so until new data is made available. If "TX automatic" mode is selected, the transmitter is also turned off during this time.

	Transmitter enabled in "TX automatic" mo de				
	Trans	mitter enabled	in "TX on"	mode	
PRNG data	TM	TM		TM	PRNG data
PRINGUALA	frame	frame	•••	frame	PRING Uala
Message	个 eis scheduled				

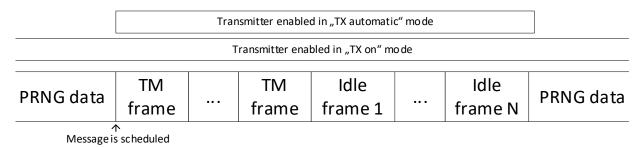
Figure 13: Transmission behaviour

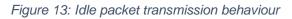
There are two additional parameters that can be used to influence this sequence. First is the "TX wait time" parameter, which specifies the amount of time to wait after data is made available and the transmitter is turned on before starting the transmission of the first TM frame.





The second parameter is the "Empty messages" parameter. This parameter defines the number of Idle Space Packet Protocol frames that are sent after the last TM frame that contains scheduled data is sent. The Idle frames are sent with one Space Packet Protocol Frame per TM frame, where the APID is set to all ones, marking it as an Idle Packet. The Sequence flags are set to 11, marking that it contains unsegmented user data. The size of the packet is fixed to 205 bytes, and all the data bytes are set to 0xe0.





If additional data is scheduled to be transmitted while the Idle packet sequence is being transmitted, the scheduled data is transmitted in the next available TM frame and the Empty messages count is reset to 0. As such, the system guarantees that for every end of transmission, a number of Idle SPP messages equal to the "Empty messages" parameter will be sent.

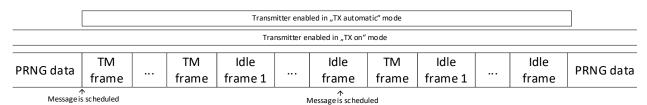


Figure 13: Interrupted idle packet transmission behaviour

For "RX on, TX off" modes and "TX on, RX off" modes, the NANOlink will never transmit any data.

For "RX on, TX unmodulated carrier" mode, the NANOlink will continuously transmit an unmodulated carrier.

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A. Appendix A

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