150-Watt CubeSat
Electrical Power System (EPS)

Technical Reference Manual

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1.1 Signatures

Prepared by: John Bevilacqua, Ibeos

Director of Engineering

_____ _____

Signature Date

Approved by: Abigail Davidson, Ibeos

Director of Programs

_____ _____

Signature Date

1.2 Revision History

Revision	Description	Date	Approval
-	Initial Release	4/1/2019	RVR
A	Updated 5V bus converter short circuit current; Updated power converter specifications to reflect further testing. Updated Switch 1 output current transfer function. Added detail to the BCR current control section. Added CRC generation code example. Reduced default maximum battery charge current. Updated solar array voltage range. Updated switch, power converters, BCR specifications based on final test results. Added timing specifications for SPI polling scheme.	4/11/2019	SHW
B	Added current limits and rise times for unswitched bus interfaces	4/23/2019	JJB
C	Corrected a sign error in the transfer function for the solar array voltage configuration register.	8/15/2019	JJB
D	Added reference efficiency plots in appendix C, added max converter capacitance limits (was TBD), adjusted limit for 12V step load voltage transient, updated SW1-5 fall time from 1 ms to 0.25ms. Added switched output parallel connection section. Updated switch 6-10 rise/fall times. Split battery bus max capacitance into unswitched bus and combined (switched plus unswitched bus).	10/24/2019	JJB
E	Updated BCR and 5V foldback current limits to 7.5A nominal; Updated BCR maximum current from 10A to 7A. Adjusted PPT voltage step size from 75 to 150 mV and slew rate from 2.25 to 4.5V/sec. Removed TBC from max BCR output capacitance. Reduced maximum 12V short circuit current from 11A to 9A. Adjusted 12V efficiency to 93.6% and 94.2% nominal. Updated Battery overcurrent Charge threshold from 16A to 14A nominal. Added recommendations for unswitched battery bus loads to ensure robust undervoltage recovery. Added BCR foldback operation details to Section 7. 30V housekeeping supply fault protection removed due to design eliminating drop-out sources that could be caused by 12V overcurrent. This removed Section 10.6, 12.6.5.3, 12.5.5, the relevant error bits in 12.5 and 12.6.6.1, and register description in 12.6.1. Added section 13.1, Thermal Considerations. Updated start-up specifications and descriptions in Section 6.3. Updated figures and tables regarding WDT resets in Section 10.7. Updated transfer function and default and max values for MBCCCR register (Section 12.6.2.2). Updated battery charge and discharge current telemetry transfer functions in Section 9.2.2. Updated battery undervoltage fault to include 3.3-Volt converter disable (Section 12.5.2). Updated latching over-current protection time to trip (Section 8.6). Moved SPI transaction timeout section beneath Timing Specification (Section 12.3.5.5). Updated SPI transaction timeout to be a byte-by-byte timeout as opposed to full-transaction timeout (See Section 12.3.5.5)	12/5/2019	JJB
F	Added Section 15 and captured errata related to the Battery Protection Fault Counter.	1/2/2020	JJB

	Updated BCR Turn-on Delay in Table 5. Updated Turn-On Time in Table 4. Updated SPI timing parameters (Min and Nominal) in Table 28. Added drop-out time for switch 1-5 SEE event in sections 3.2 and 8,2 Updated Table 6, Regulated Bus Power Converter Specs, 3.3V parameter values.		
G	Updated switch turn-on delay time in 8.2 from ~5 ms to ~2 ms		JJB

2 ACRONYMS

EPS	Electrical Power System
DC	Direct Current
AC	Alternating Current
CC&DH	Command, Control, and Data Handling
MPPT	Maximum Power Point Tracking
BCR	Battery Charge Regulator
CCA	Circuit Card Assembly
ICD	Interface Control Document
SEE	Single Event Effects
TID	Total Ionizing Dose
ESD	Electrostatic Discharge
FOD	Foreign Object Debris
TLM	Telemetry
ADC	Analog to Digital Converter
MUX	Multiplexer
SA	Solar Array
MPP	Maximum Power Point
SPI	Serial Peripheral Interface
I2C	Inter-Integrated Circuit
EoC	End-of-Charge
ESR	Equivalent Series Resistance
LSB	Least Significant Bit
LSOCR	Latching Current Limited Switched Outputs Control Register
NLSOCR	Non-Latching Current Limited Switched Outputs Control Register
SVTBA	System Voltage Telemetry Bank A
SCTBA	System Current Telemetry Bank A
SCTBA	System Current Telemetry Bank B
TTBA	Temperature Telemetry Bank A
EWRMR	External Watchdog Reset Mode Register
EWCFR	External Watchdog Configuration Register
EWCTR	External Watchdog Control Register

3 INTRODUCTION

3.1 Document Purpose

This document intends to provide all information necessary to implement this system in a spacecraft-level assembly. It describes the specifications of the system, system handling and storage guidelines, the electrical power interfaces, the CC&DH interfaces, and system testing guidelines. Note that the EPS ICD is the sole reference for specifications and recommendations regarding connector locations, mass, and mechanical and thermal interface considerations.

3.2 System Overview

The Ibeos 150-Watt CubeSat Electrical Power System is a radiation-tolerant and reliable power conditioning and distribution system with comprehensive system-wide fault tolerance. The high-level features of the EPS include:

- Full system radiation tolerance up to 30 kRad(Si) TID, operating through SEEs with an LET of up to 37 MeV-cm^2/mg and surviving SEEs with an LET of up to 55 MeV-cm^2/mg.
    - Switched outputs 1-5 can have short interruptions due to SEE events, but will not turn-on due to an SEE
- Efficient solar array power conversion and battery charging via single-input maximum power point tracker with a 7A rated output current
- Overall power handling capability of up to 150W
- Regulated 12-Volt, 5-Volt, and 3.3-Volt outputs
- Unregulated battery bus outputs
- 10 switched power outputs
    - 8x solder-jumper-configurable to 3.3-Volt, 5-Volt, 12-Volt or unregulated battery busses
        - 4 with slow rise time, current telemetry, and latching over-current protection
        - 4 with fast rise time
    - 2x unregulated battery power for battery heaters
- Unswitched power outputs
- SPI and I2C CC&DH interface for system commanding, control, and telemetry acquisition
- Spacecraft-level configurable watchdog timer via CC&DH interface

3.3 Block Diagram

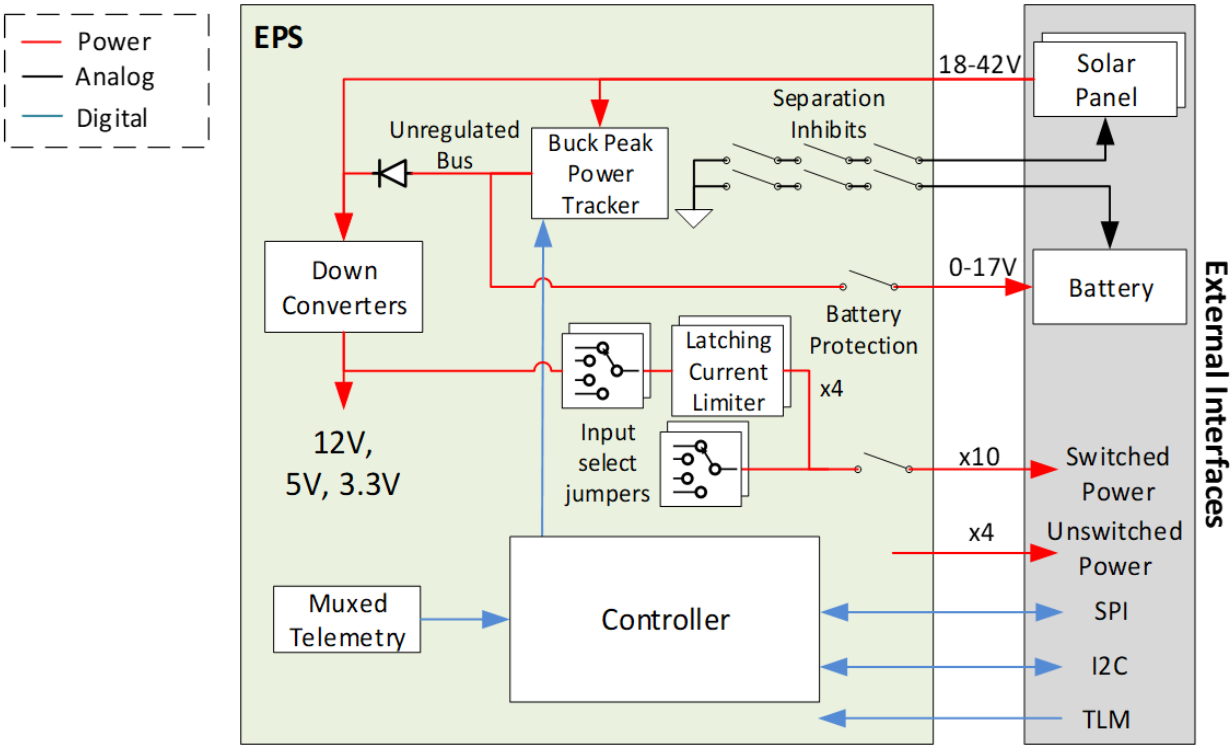


Figure 1. EPS Functional Block Diagram

4 HANDLING AND STORAGE GUIDELINES

The specific handling and storage guidelines for the EPS are included below. Failure to follow these guidelines may result in damage to the EPS hardware or degradation in system performance.

4.1 General Handling

During all handling of the EPS system, care must be taken to keep the system clear of any contaminants, both conductive and non-conductive. Foreign object debris can create circuit shorts which can permanently alter system performance even after the FOD is removed.

Caution: When integrated with a battery, extra caution must be taken to not short terminations that have un-fused battery power on them. Failing to do so may result in hazards.

It is recommended that gloves we worn when handling EPS flight units to minimize the transfer of oils and outgassing materials.

It is recommended that flight units be removed from the delivery packaging and handled only in a cleanliness-controlled environment.

4.2 Electro-Static Discharge

The EPS implements several electronic devices that are sensitive to ESD and therefore the circuit card must only be handled in a static-dissipative environment with proper ESD protective equipment.

4.3 Storage

The EPS is delivered in anti-static packaging with a hygroscopic drying agent to keep the relative humidity of the packaged system very low. Upon receipt of EPS units, it is recommended that they be stored in an anti-static, humidity-controlled environment with a temperature between 20°C and 40°C. In this environment, the EPS can be stored for up to 3 years.

5 SYSTEM SPECIFICATIONS

5.1 Absolute Maximum Operating Conditions

Table 1. Absolute Maximum Operating Conditions

Parameter	Min	Max	Units
Solar Array Voltage	0	42	V
Battery Voltage	0	19	V
Card Interface Temperature	-35	70	°C

5.2 Recommended Operating Conditions

Table 2. Recommended Operating Conditions

Parameter	Min	Max	Units
Solar Array Voltage	19	40	V
Battery Voltage	13.2	16.8	V
Card Interface Temperature	-25	60	°C

5.3 Specifications

Unless otherwise noted, the conditions in the table below apply to the specification in this section.

Table 3. Default Conditions for EPS Specifications

Parameter	Value	Units
Card Interface Temperature	25	°C
SA MPP Voltage, $V_{SA,MPP}$	24	V
Battery Voltage, V_{Batt}	16	V

5.4 General Specifications

Table 4. General Specifications

Parameter	Conditions	Min	Nom	Max	Units
Quiescent Power Consumption	Switched outputs off, V_{Batt}=16 V, V_{SA}=40 V	-	1.4	-	W
Quiescent Power Consumption	Switched outputs off, V_{Batt}=16 V, V_{SA}=0 V	-	1.1	-	W
Quiescent Power Consumption	Undervoltage, V_{Batt}=16 V, V_{SA}=40 V	-	0.9	-	W
Quiescent Current	Any inhibit closed, V_{Batt}=16 V	-	0.2	0.3	mA
Quiescent Current	Undervoltage active V_{Batt}=10 V, V_{SA}=0 V	-	6	8	mA
Solar Array Current per Pin	-	0	1	2	A

Parameter	Conditions	Min	Nom	Max	Units
Turn-On Time	Time from inhibit released to accepting commands	-	400	-	msec
Mass	CCA only; not including Wedge-Loks, etc.	-	140	-	g

5.4.1 Battery Charge Regulator (BCR) Specifications

Table 5. BCR Specifications

Parameter	Conditions	Min	Nom	Max	Units
Battery Voltage	Operating	13.2	-	16.8	V
Charge Current Ripple	Charging	-	45	-	mA
Battery Charge Current		See Section 12.6.2.2			
Efficiency	Excludes EPS quiescent current, 5 A out	93	95	96.5	%
Output Current Limit	Charge current plus battery bus loading	-	-	7	A
Overcurrent Limit	Foldback	-	7.5	-	A
MPPT Slew rate	-	-	4.5	-	V/sec
MPPT Step Size	-	-	150	-	mV
Battery Bus Voltage, Protection Mode	No battery connected or during overvoltage protection	-	21	-	V
Default V_{SA}	Peak power tracking disabled	-	19	-	V
Turn-on Delay	Time from power applied to BCR providing current	-	990	-	msec
Charge Current Refresh Rate	-	-	30	-	Hz
V_{SA} Refresh Rate (peak power tracking)	-	-	30	-	Hz
Charge Current Step Size		-	45	-	mA
Maximum output capacitance	Battery bus unswitched outputs (external)	-	100	-	uF
Maximum output capacitance	Combined battery bus switched and unswitched outputs (external)	-	500	-	uF

5.4.2 Regulated Bus Power Converter Specifications

Table 6. Regulated Bus Power Converter Specifications

Parameter	Conditions	Min	Nom	Max	Units
12V Converter					
Output Voltage	DC	11.6	12.1	12.4	V
Output Voltage	DC + AC	10.8	-	13.2	V

Parameter	Conditions	Min	Nom	Max	Units
Efficiency, Battery Input	Excludes EPS quiescent current, 3 A out, V_{SA}=0 V	91	93.6	95.5	%
Efficiency, Solar Array Input	Excludes EPS quiescent current, 3 A out, V_{SA}=30 V	93	94.2	95.5	%
Output Ripple Voltage (ac)	-	-	10	50	mV
Transient Response	0 A to 1.5 A	-300	150	-	mV
Transient Response	1.5 A to 0 A	-	150	-300	mV
Rise Time	-	1	4	10	msec
Output Current	-	0	-	4	A
Short Circuit Current	-	5	7	9	A
Load Capacitance	External to unit, all switched and unswitched 12V outputs combined	0	-	500	uF
5V Converter					
Output Voltage	DC	4.75	5.0	5.25	V
Output Voltage	DC + AC	4.5	5.0	5.5	V
Efficiency, Battery Input	Excludes EPS quiescent current, 5 A out, V_{SA}=0 V	88	91	92	%
Efficiency, Solar Array Input	Excludes EPS quiescent current, 5 A out, V_{SA}=30 V	90	92	94	%
Output Ripple Voltage (AC)	-	-	10	50	mV
Transient Response	0 A to 3 A	-150	-75	-	mV
Transient Response	3 A to 0 A	-	75	150	mV
Rise Time	-	1	10	30	msec
Output Current	-	0	-	6	A
Short Circuit Current	-	6.5	7.5	9	A
Load Capacitance	External to unit	0	-	1000	uF
3.3V Converter					
Output Voltage	DC	3.15	3.3	3.45	V
Output Voltage	DC + AC	3	3.3	3.6	V
Efficiency	Excludes EPS quiescent current, 3 A out, V_{SA}=0 V	88	91	94	%
Output Ripple Voltage (ac)	-	-	10	50	mV
Transient Response	0 A to 1.5 A	-200	-50	-	mV
Transient Response	1.5 A to 0 A	-	50	150	mV
Rise Time	-	1	10	30	msec
Output Current	-	0	-	3	A
Short Circuit Current	-	6	7	9.5	A
Load Capacitance	External to unit	0	-	1000 [TBC]	uF

5.4.3 Switched Output Specifications

Table 7. Switched Output Specifications

Parameter	Conditions	Min	Nom	Max	Units
Switched Outputs 1-5					
Rise Time	-	0.5	1	2	msec
Fall Time	-	-	0.25	-	msec
SW 1 Current (Note 1)	-	-	-	6	A
SW 2 Current (Note 1)	-	-	-	4.5	A
SW 3 Current (Note 1)	-	-	-	3	A
SW 4 Current (Note 1)	-	-	-	3	A
SW 5 Current	-	-	-	2	A
Switched Outputs 6-10					
Rise Time	-	0.03	-	0.3	msec
Fall Time	-	-	5	-	msec
SW 6-10 Current	-	-	-	2	A

1. If output is configured to provide 3.3-Volt or 12-Volt power, the maximum output current is limited by the converter current limit (listed above). These limits may be further bounded by latching current limits.

5.4.4 Unswitched Output Specifications

Table 8. Switched Output Specifications

Parameter	Conditions	Min	Nom	Max	Units
Unregulated Bus					
Rise Time	Exiting undervoltage	-	TBD	-	msec
Rise Time	Separation Inhibit Release	-	TBD	-	msec
Maximum Current, DC	I/O limited	-	-	12	A
Maximum Current, transient	<1 ms duration	-	-	24	A
12V Bus					
Rise Time		-	5	-	msec
Maximum Current, DC	I/O limited	-	-	2	A
Maximum Current, transient	<1 ms duration	-	-	4	A
5V Bus					
Rise Time		-	16	-	msec
Maximum Current, DC	I/O limited	-	-	2	A
Maximum Current, transient	<1 ms duration	-	-	4	A
3.3V Bus					
Rise Time		-	1	-	msec
Maximum Current, DC	I/O limited	-	-	2	A
Maximum Current, transient	<1 ms duration	-	-	4	A

5.4.5 Fault Protection Specifications

Table 9. Fault Protection Specifications

Parameter	Conditions	Min	Nom	Max	Units
Battery Under-Voltage Threshold	Falling	12.4	12.7	12.9	V
Battery Under-Voltage Threshold	Rising	13.7	14.25	14.7	V
Battery Over-Voltage Threshold	Rising	16.9	17.3	17.55	V
Battery Over-Voltage Threshold	Falling	16.7	17.1	17.4	V
Battery Over-Current Charge Threshold	-	12	14	16	A
Battery Over-Current Discharge Threshold	-	25	33	37	A
Sw. 1 Over-Current Threshold (Note 1)	-	2.5	3	3.5	A
Sw. 2 Over-Current Threshold (Note 1)	-	4.05	4.5	4.95	A
Sw. 3 Over-Current Threshold (Note 1)	-	2.7	3	3.3	A
Sw. 4 Over-Current Threshold (Note 1)	-	2.7	3	3.3	A

1. Latching current limits are configurable at time of order. See Appendix B: Software Configurable Parameters.

5.4.6 Spacecraft Watchdog Specifications

Table 10. Spacecraft Watchdog Specifications

Parameter	Conditions	Min	Nom	Max	Units
No Pet Trip Duration (System Safed)	Default is 128 sec	1	128	130	sec
Post-Trip System Reset Duration	Non-Global	0.5	1.2	1.5	sec
Post-Trip System Reset Duration	Global	6	-	11	sec

5.4.7 Housekeeping Specifications

Specifications in this section are for reference only. These pertain solely to internal card functionality.

Table 11. Housekeeping Specifications

Parameter	Conditions	Min	Nom	Max	Units
3.3-Volt Housekeeping Supply Voltage	-	3.0	3.3	3.6	V
12-Volt Housekeeping Supply Voltage	-	9	11.3	12	V
30-Volt Housekeeping Supply Voltage	-	24	28.5	33	V

5.4.8 Internal Watchdog Specifications

Table 12. Internal Watchdog Specifications

Parameter	Conditions	Min	Nom	Max	Units
Internal Watchdog Trip Time	-	-	3	-	sec
Internal Watchdog Reset Duration	-	-	6	-	sec

6 SYSTEM INITIALIZATION

6.1 Spacecraft Inhibits

The spacecraft inhibits are low side series switches that open the connection between both the battery and system ground as well as the solar array and system ground. The only ground path for the battery is through the inhibit switches. The inhibit circuits are single-fault tolerant. The battery and solar array low side inhibits are separate switches in order to ensure that the inhibited EPS provides two-fault tolerance with respect to either powering the spacecraft or charging the battery.

The simplified block diagram below shows the inhibit configuration. The following circuit elements shown are simplified for readability:

- Current sense circuits are not shown
- Gate bias resistor is a simplification of the bias circuit
- The gate-source bleed resistors and timing capacitors are not shown

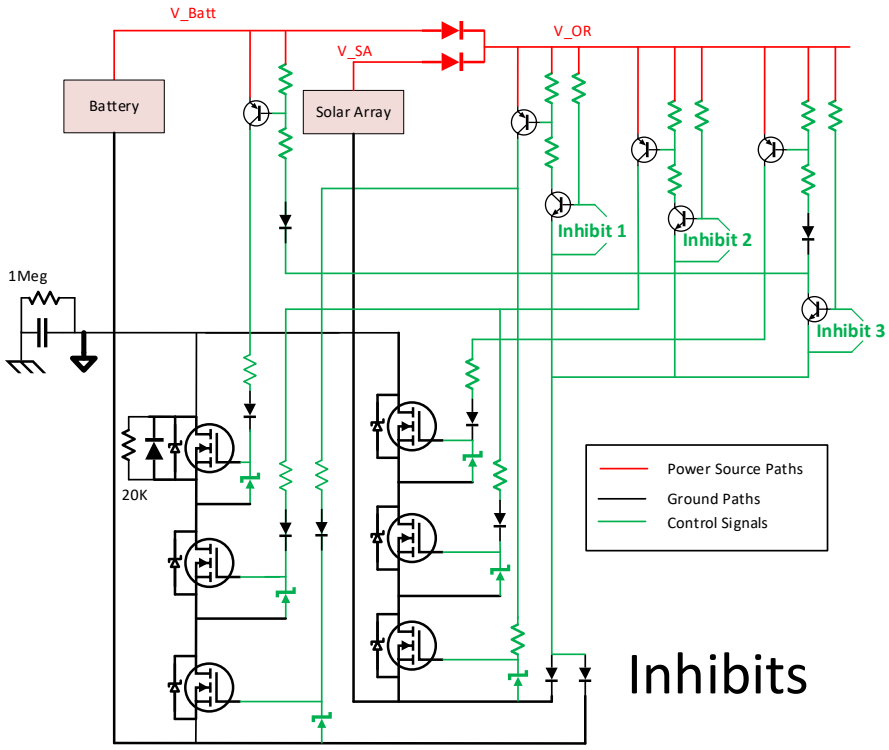


Figure 2. Simplified Spacecraft Inhibits Schematic

6.2 Separation Switches

The spacecraft inhibits, as described in Section 6.1, are to be driven by separation switches. The separation switches are not a part of the EPS CCA. A single separation switch is to be connected across a given INHIBIT_n_P1/INHIBIT_n_P2 pair on the J3 connector. See Section 11.2 for connector pin assignments for the 3 pairs of signals. If fewer than 3 separation inhibits are

needed, the unused separation inhibit pins should be left unconnected (open). Separation inhibits should never be connected in parallel with each other or any other connection.

The separation switches behave per Table 13 below.

Table 13. Separation Switch Logic

Inhibit	Signal Names	Sep. Switch State	Inhibit State
1	INHIBIT_1_P1, INHIBIT_1_P2	Closed	Asserted
		Open	Released
2	INHIBIT_2_P1, INHIBIT_2_P2	Closed	Asserted
		Open	Released
3	INHIBIT_3_P1, INHIBIT_3_P2	Closed	Asserted
		Open	Released

6.3 EPS Start-Up

6.3.1 Normal Start-up

The normal EPS start-up is a sequenced event. First the 3.3-Volt and 12-Volt housekeeping supplies become valid. At this point, all switching power converters are disabled. The microcontroller then goes through the following start-up sequence:

Figure 3. Normal EPS Start-Up Sequence

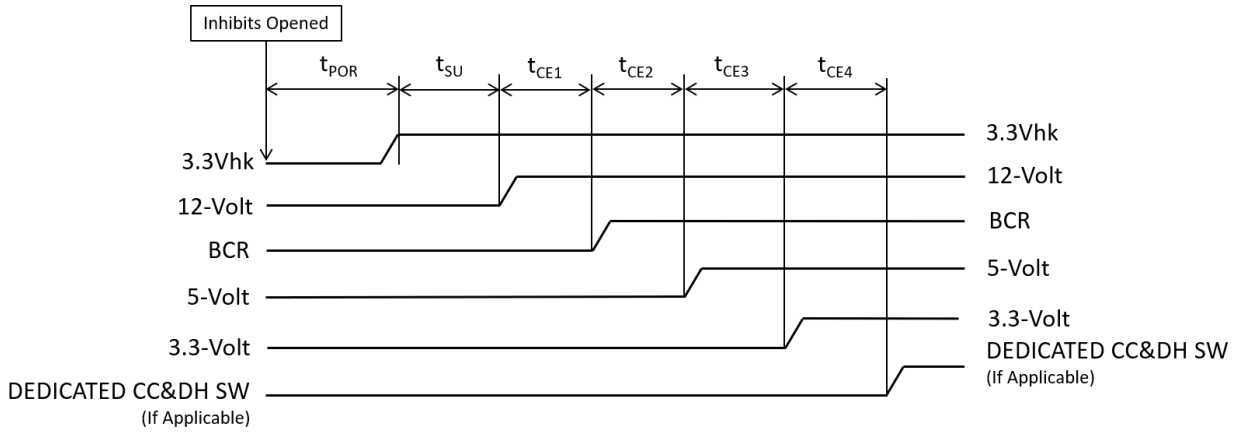


Table 14. Normal EPS Start-Up Sequence Timing Parameters

Symbol	Parameter	Condition	Min	Nom	Max	Units
t_{POR}	MCU Power-on-Reset Duration	–	–	5	–	ms
t_{SU}	MCU Initialization Duration	–	–	20	–	ms
t_{CE1}	Converter Enable Command Sequence Interval, 12-Volt	–	–	25	–	ms
t_{CE2}	Converter Enable Command Sequence Interval, BCR	–	–	185	–	ms
t_{CE3}	Converter Enable Command Sequence Interval, 5-Volt	–	–	90	–	ms

Symbol	Parameter	Condition	Min	Nom	Max	Units
t_{CE4}	Converter Enable Command Sequence Interval, 3.3-Volt	–	–	20	–	ms

1. Timing values are taken at ambient temperature with no external loads.

Note: The unregulated battery bus might come up prior to the 12-Volt output if insufficient solar array power is available when the inhibits open.

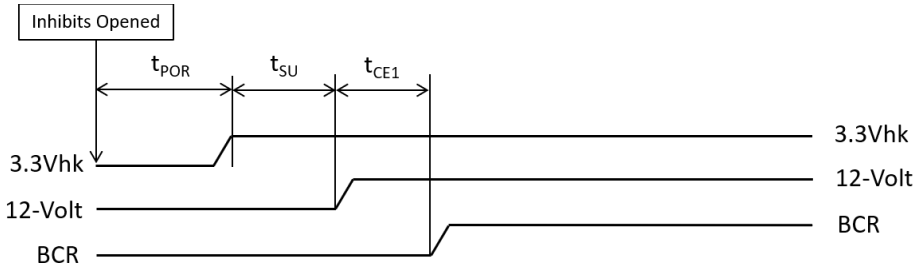
Following the start-up sequence, the EPS will enter its normal routine which consists of executing several periodic functions including:

- Battery charge regulation
- Solar array power regulation
- Fault detection and recovery
- Telemetry acquisition and serialization
- Flight computer communication

6.3.2 Start-up During Battery Undervoltage

The EPS will attempt to start-up whenever the inhibits are released and the battery is above the rising UVP limit. If the battery is below the UVP limit, the EPS will enter a low current state until either the voltage at the battery interface rises or power is available from the solar array interface. Once solar array power is available, the EPS will go through the following start-up sequence:

Figure 4. EPS Undervoltage Start-Up Sequence Phase 1



After enabling the BCR, the EPS will enter its normal routine, as described above, with the following variance(s):

1. Charge the battery at the default charge current, fixed solar array voltage, and EoC battery voltage.

When the battery voltage reaches the rising undervoltage threshold, the EPS will go through the remainder of the start-up sequence as depicted below:

Figure 5. EPS Undervoltage Start-Up Sequence Phase 2

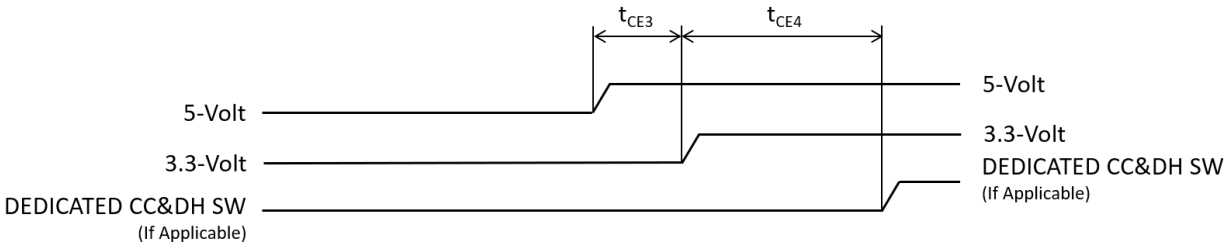


Table 15. EPS Undervoltage Start-Up Sequence Timing Parameters

Symbol	Parameter	Condition	Min	Nom	Max	Units
t_{POR}	MCU Power-on-Reset Duration	–	–	5	–	ms
t_{SU}	MCU Initialization Duration	–	–	20	–	ms
t_{CE1}	Converter Enable Command Sequence Interval, 12-Volt	–	–	25	–	ms
t_{CE3}	Converter Enable Command Sequence Interval, 5-Volt	–	–	90	–	ms
t_{CE4}	Converter Enable Command Sequence Interval, 3.3-Volt	–	–	20	–	ms

1. Timing values are taken at ambient temperature with no external loads.

Note: The unregulated battery bus might come up prior to the 12-Volt output if insufficient solar array power is available when the inhibits open.

If the available solar array power is low, it may take significant time until the 5-Volt, 3.3-Volt, and dedicated CC&DH switched output (if applicable) are enabled/closed. If the spacecraft is tumbling, it will repeat the sequence in Figure 4 until the battery undervoltage circuit releases.

If the battery is in undervoltage and solar array power is insufficient to supply the quiescent power of the EPS card, it will exhibit a cyclic behavior in which its housekeeping circuits turn on and it begins to sequence up the power converters. The inrush current of the power converters will then cause the solar array voltage to sag. This sag will cause the power converters to turn off due to the housekeeping voltages falling out of regulation. This cycle will repeat until either the available solar array power increases (or the solar array power falls further).

Any loads on the unswitched battery bus should be selected such that they do not cause lock-up during an undervoltage recovery by putting the Battery Charge Regulator into foldback at low voltage. An example of a load that could do this is a constant power converter that operates down to very low voltage. If the converter consumed 40W of power when the BCR output voltage is at 5V, the BCR would be in foldback and unable to provide current to the battery. Undervoltage limits on any constant power unswitched battery bus loads are highly recommended. Unswitched load should be selected that can start up with a constant current source.

7 BATTERY CHARGE REGULATOR

The battery charge regulator (BCR) provides power to the battery bus from the solar array. It operates as a downconverter. The input voltage must be at least 10% (approximately) above the battery voltage for it to provide current.

The battery charge regulator operates in two normal modes: battery current control and solar array voltage control as well as an abnormal current foldback mode.

7.1 Battery Current Control

The BCR net battery current is commanded by the EPS microcontroller. The commanded current is based on the EoC voltage, battery voltage, and the maximum allowable charge current. The end of charge voltage and maximum allowable charge current are software-controlled parameters that may be adjusted via writes to the following registers.

0x10 - Battery End of Charge Voltage (EOCV) Configuration Register

0x11 - Maximum Battery Charge Current Configuration Register

The microcontroller will reduce the commanded current when the measured voltage on the EPS card reaches the EoC voltage to perform a taper charge. Battery voltage is measured locally and will include drops due to the series resistance between the EPS card and the battery along with the internal ESR of the battery.

The commanded battery current can be set to negative values down to approximately -2 A (2-Amp discharge) in order to ensure that the battery can be float charged even if there is an offset error in the telemetry.

The microcontroller updates the commanded battery charge current at 30 Hz. Each update can increase or decrease the commanded current by a single 45 mA step. When the maximum commanded current is increased and sufficient power is available, the battery current will increase in 45 mA steps at 30 Hz up to the new maximum. When the maximum commanded current is decreased and the BCR current loop is in control, the battery current will quickly fall (in less than 200 ms) to the new maximum. The rate of this decrease in current is driven by the BCR hardware control loop.

7.2 Solar Array Voltage Control

7.2.1 Constant Voltage Regulation Mode

At start-up, SA voltage control is in a constant voltage regulation mode at a solar array voltage of 19 V. While in this mode, the MCU will command the SA voltage to the value specified by the following configuration register:

0x12 – Solar Array Voltage Configuration Register

The SA voltage control mode is changed between available modes by writing to the following register:

0x35 – Peak Power Tracker Control Register

7.2.2 Maximum Peak Power Tracking Mode

When MPPT mode is enabled and the measured battery charge current is below the commanded battery charge current (i.e. the solar array is not providing the desired amount of power), the MPPT algorithm takes control and drives the BCR set point. The BCR is put into MPPT mode via the following register:

0x35 – Peak Power Tracker Control Register

In MPPT mode, the microcontroller uses a hill-climbing algorithm to find the maximum operating power point of the solar array. The microcontroller calculates solar array power then commands the solar array voltage up or down by one 75 mV step. After taking the step, the new solar array power is calculated and compared to the previous calculation. If the new power is higher, the microcontroller will take another step in the same direction. If the new power is lower, the microcontroller will take a step in the opposite direction. This results in a steady-state behavior in which the solar array walks around the maximum power point with the operating voltage ranging between one step above and one step below the maximum power point (i.e. there will be three observed operating points). If there is significant noise in the system or the change in current is less than one LSB, the peak power tracker may take somewhat longer to adjust to the peak power point.

If the measured solar array current gets below 100 mA, the microcontroller will command the solar array to the default solar array voltage. From there the peak power tracking algorithm will again climb the power slope of the solar array until it reaches a global or local maximum.

It is not recommended to use solar array strings with different numbers of cells as that can create local maxima. If the solar array has more than one maxima, the setpoint can be commanded above them by:

1. Entering constant voltage regulation mode
2. Setting the minimum solar array voltage to a level above the local maxima
3. Enabling MPPT mode

Note: When there is no solar array power, the BCR will operate at zero duty cycle due to the solar array voltage being below the minimum commanded voltage.

7.3 Power Supply Interface Power Transients

The BCR power converter operates with a voltage mode controller inner loop. As a result, significant changes in the input power supply can generate transient currents and voltages on the output while the feedback amplifiers adjust to the new operating conditions.

If the EPS is connected to a high ESR load on the battery interface such as an electronic load operating in constant voltage mode, this may cause nuisance trips on the battery fault protection circuits. It is recommended that a large capacitance be added in parallel with an electronic load if the EPS is being operated without an actual battery.

7.3.1 BCR Foldback

When the BCR output current is commanded to be above 7.5A (nominal value) with a solar array capable of supplying that power into the BCR via a combination of charge current and battery bus loads, the converter will enter a current limit mode in order to provide thermal protection of the main switching devices. This limit was selected based on thermal testing that showed operation within de-rated limits with the board thermal interface temperature near the 70 degree C qualification level and a high overall board power dissipation configuration. The limit varies somewhat with solar array voltage with a typical limit of 7.5A at 19V and 8.1A at 40V.

In some instances, operating with the BCR in foldback current limit while the solar array is operating near or at the peak power point can cause the BCR to transition between the foldback limit and voltage mode regulation. This is not stressful to the BCR, but can cause higher ripple currents and voltages on the solar array and battery, as well as reduce the efficiency of the solar array due to the variation of the operating voltage. If this is observed, it can be avoided by reducing the commanded battery charge current such that the BCR is not operating in foldback or other configuration adjustments that either increase the solar array power to above the BCR foldback limit or reduce the BCR current to below the foldback limit.

8 SWITCHED OUTPUTS

8.1 Overview and Configurability

The EPS has 10 switched outputs. At time of manufacture, switched outputs 1-8 can each be configured to switch either 3.3V power, 5V power, 12V power, or unregulated battery power. Switched outputs 9 and 10 switch unregulated battery power and are dedicated to outputs for battery heaters 1 and 2, respectively.

8.2 Switched Output Operation

The EPS's switched outputs are commandable via register writes over the CC&DH interface. The following registers are relevant to switched output commanding:

- *0x31 – Latching Current Limited (LCL) Switched Outputs Control Register*
  - This register contains the switch state bits for switched outputs 1-4 as well as the respective over-current trip indicator bit for each switch.
  - See Section 12.6.3.2 for details on register utilization.
- *0x32 – Non-Latching Current Limited Switched Outputs Control Register*
  - This register contains the switch state bits for switched outputs 5-10.
  - See Section 12.6.3.3 for details on register utilization.

By default, switched outputs 1-10 are all open. If a designated CC&DH switched output is configured, the default output is Switch 5 (SW5). If configured, this switch is powered on as part of the system start-up sequence. See Section 6 for details regarding the start-up sequence.

A given switch is closed by writing the relevant switch state bit in the LSOCR or the NLSOCR as a 1. Conversely, a given switch is opened by writing the relevant switch state bit in the LSOCR or the NLSOCR as a 0. When writing to a given switch control register, the changes take effect immediately after reception of a valid write command.

Switches that are closed must have their state bit written as a 1 during future writes if the switch is to stay closed. Switches that are open must have their state bit written as a 0 during future writes if the switch is to stay open.

Writing SW5 open, when configured as the dedicated CC&DH output, is an illegal command that will be ignored. If commanding other switches in the same control register as SW5, write the relevant SW5 bit as a 1. Failing to do this will result in the command being ignored and an "Illegal Command" response being returned.

If state changes for multiple switches are commanded via the same register write command, the following sequence is followed:

1. Switches to be opened are all simultaneously opened
2. Switches to be closed are sequenced on by state bit order (lowest-order bit to highest-order bit)

Figure 6 below depicts this sequencing. The scenario depicted is an NLSOCR value of 0x00 that is rewritten as 0x0B followed by 0x01 and then by 0x0A.

Figure 6. Switched Output Command Timing Diagram

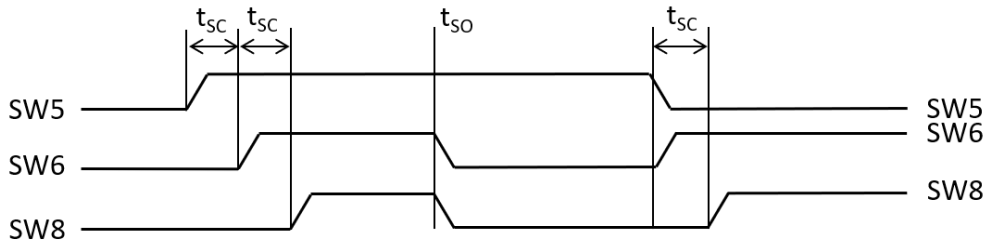


Table 16. LSOCR Switched Output Command Timing Parameters

Symbol	Parameter	Condition	Min	Max	Units
t_{SC}	Switch Close Command Sequence Interval	-	1	–	ms
t_{SO}	Switch Open Command Sequence Interval (Note 1)	-	–	0	ms

1. All switches written open via the same register write command will be opened at the same time.

Each switch has a SEE filter that prevents an upset on the microcontroller from causing an inadvertent turn-on. This filter also results in there being an ~2 ms second delay between the time when the turn-on/off command is sent from the microcontroller to the start of the switch rise time. This delay can vary by several milliseconds and is in addition to the delay that the microcontroller uses to stagger switch inrush currents.

Switches 6-10 are immune to SEE induced turn-off for SEE levels below 37 MeV-cm^2/mg. Switches 1-5 can have a drop-out of up to 2 ms due to an SEE event.

8.3 Switched Output Rise/Fall Time

Switched outputs 1-5 have enhanced rise time control in order to reduce the inrush current for capacitive loads. These switches have a slow rise time and a fast fall time, relatively. Switched outputs 6-10 have a fast rise time and a slow fall time, relatively.

See Section 5.4.3 for relevant switched output specifications.

8.4 Switched Output Insertion Loss

Switched outputs typically have approximately 20-40 mΩ of series resistance depending on the temperature of the EPS card. It is not recommended to have more than 8 A DC current on any switched output.

8.5 Switched Output Inrush Transients

The regulated voltages are current limited by the pulse-by-pulse limit of the 3.3-V, 5-Volt, and 12-Volt power converters. Very high load capacitances may cause there to be sag on the switched output if there is not inrush current limiting on the load. This is a result of the power converters peak current limiting circuits. If there is especially high capacitance on an output, turning that

output on while the power converter is operating at lower current will help minimize voltage sag. If the total current on an power converter output is below 50% of the rated maximum when an output is turned on, the maximum recommended switched output capacitance can be increased. The recommended maximum output capacitance for each switch type is listed in Table 17.

Table 17. Recommended Maximum Switched Output Capacitance

Output Voltage	Max. Capacitance (SW1-5)	Max. Capacitance (SW6-10)	Max. Capacitance (SW1-5)	Max. Capacitance (SW6-10)
	<50% rated output current		<100% rated output current	
3.3 V	400 uF	120 uF	200 uF	100 uF
5.0 V	400 uF	120 uF	200 uF	100 uF
12.0 V	200 uF	47 uF	100 uF	39 uF
Battery	400 uF	47 uF	200 uF	39 uF
Heater	N/A	1 uF	N/A	1 uF

8.6 Latching Over-Current Protection

The microcontroller monitors current telemetry for switches 1-4 at a rate of 500 Hz to determine whether any switch is carrying more than its limit. If the measured current exceeds the limit for two or more consecutive samples, the microcontroller sets an overcurrent error status bit for the switch in question and commands the switch open. It takes 7 +/-4 milliseconds from the start of an overcurrent event until the switch opens. The delay is due to the sample rate, consecutive samples, SEE filter delay, and the switch's fall time.

In order to turn on a switch that has experienced an overcurrent event, a command must be sent to clear the overcurrent error prior to or simultaneous with the switch turn-on command.

See Section 12.6.3.2 for more information regarding the over-current flags and control of the latching current limited outputs.

8.7 Parallel Connection of Switched Outputs

Switched outputs should not be connected in parallel without consulting Ibeos. The circuit used to enhance turn-off time can have higher than normal dissipation if a DC voltage is applied to it and may result in overstress to the components.

9 TELEMETRY

9.1 Overview

The EPS provides 10-bit telemetry for all the key analog voltages, currents, and temperatures on the card. All telemetry measurements are accessible over the CC&DH interface via a master telemetry read command and are organized across the following telemetry banks:

- *0x50 – System Voltage Telemetry Bank A*
  - This telemetry bank contains all available voltage telemetry points.
  - See Section 12.6.4.1 for details on this bank.

- *0x52 – System Current Telemetry Bank A*
  - This telemetry bank contains a sub-set of all available current telemetry points.
  - See Section 12.6.4.3 for details on this bank.
- *0x53 – System Current Telemetry Bank B*
  - This telemetry bank contains the balance of all available current telemetry points that are not included in SCTBA.
  - See Section 12.6.4.4 for details on this bank.
- *0x54 – Temperature Telemetry Bank A*
  - This telemetry bank contains all available temperature telemetry points.
  - See Section 12.6.4.6 for details on this bank.

All 10-bit telemetry points are represented and transmitted over the CC&DH interface as digitized voltages. The following section details how to translate such digital values into the analog measurements that they represent.

9.2 System Telemetry Transfer Functions

9.2.1 Analog Voltage Conversion

A 10-bit digital telemetry point shall be converted to its equivalent analog voltage using the following equation:

$$V = X * 2.50/1024 \quad \text{Eq. 1}$$

where:

V is the equivalent analog voltage
X is the 10-bit digital telemetry value

Given this analog voltage between 0V and 2.50V, the linear transfer functions in Section 9.2.2 shall be used to convert this value to the real measurement it represents.

9.2.2 Linear Transfer Functions

The following equation shall be used to convert the analog voltage ('V' from Section 9.2.1) to its equivalent real measurement:

$$T = M \times V + B \quad \text{Eq. 2}$$

where:

T is the real measurement
V is the analog voltage from Eq. 1
M is the slope (per following tables)
B is the Y-intercept (per following tables)

The tables below provide an M and B value for each telemetry point.

9.2.2.1 SVTBA Transfer Function Inputs

Table 18. SVTBA Transfer Function Inputs

TLM POINT	LABEL	SLOPE	Y-INTERCEPT
7	Solar Array Voltage	21.000	0.000
6	Battery Bus Voltage	11.000	0.000
5	5V Converter Output Voltage	3.004	0.000
4	12V Converter Output Voltage	6.100	0.000
3	3.3V Housekeeping Voltage	2.000	0.000
2	12V Housekeeping Voltage	6.100	0.000
1	30V Housekeeping Voltage	21.000	0.000
0	3.3V Converter Output Voltage	2.000	0.000

9.2.2.2 SCTBA Transfer Function Inputs

Table 19. SCTBA Transfer Function Inputs

TLM POINT	LABEL	SLOPE	Y-INTERCEPT
7	Solar Array Current	4.902	0.000
6	Battery Charge Current	3.887	-1.961
5	5V Converter Output Current	4.902	0.000
4	12V Converter Output Current	2.128	0.000
3	Switched Output 1 Current	5.319	0.000
2	Switched Output 2 Current	2.128	0.000
1	Switched Output 3 Current	2.128	0.000
0	Switched Output 4 Current	2.128	0.000

9.2.2.3 SCTBB Transfer Function Inputs

Table 20. SCTBB Transfer Function Inputs

TLM POINT	LABEL	SLOPE	Y-INTERCEPT
7	Battery Discharge Current	20.120	-10.040
6	3.3V Converter Output Current	2.128	0.000
5	N/A	N/A	N/A
4	N/A	N/A	N/A
3	N/A	N/A	N/A
2	N/A	N/A	N/A
1	N/A	N/A	N/A
0	N/A	N/A	N/A

9.2.2.4 TTBA Transfer Function Inputs

Table 21. TTBA Transfer Function Inputs

TLM POINT	LABEL	Thermistor Part Number
7	System Temperature	B57621C5103J062 4.99 kΩ 0.01% pull up to 2.50 V
6	Solar Array Temperature B	Customer Furnished Thermistor 4.99 kΩ 0.01% pull up to 2.50 V
5	Solar Array Temperature A	Customer Furnished Thermistor 4.99 kΩ 0.01% pull up to 2.50 V
4	Battery Temperature B	Customer Furnished Thermistor 4.99 kΩ 0.01% pull up to 2.50 V
3	Battery Temperature A	Customer Furnished Thermistor 4.99 kΩ 0.01% pull up to 2.50 V
2	N/A	N/A
1	N/A	N/A
0	N/A	N/A

9.3 Telemetry Error

9.3.1 Analog Circuit Error

Due to component tolerances, leakage currents, and input offsets, each telemetry point will have a slight error factor. If tighter telemetry measurements are required, the delivered test data for a given flight unit may be used to tune out measurement offsets.

Typical full-scale telemetry accuracy over temperature and mission life is within +/-1% for voltage telemetry and +/-3% for current telemetry.

Telemetry values are gathered automatically by the EPS card at a rate of 30 Hz. The telemetry points in a given sample may be gathered up to 33 ms before a telemetry packet is sent. The telemetry points within a packet may also have been gathered up to 33 ms apart.

9.3.2 Single Event Effects

There is the potential for the analog-to-digital converter implemented within the system to upset due to single event effects. Such an upset has the potential to cause an erroneous telemetry value.

Recommendation: Due to the SEE susceptibility of the EPS ADC, it is recommended that action never be taken on a single telemetry measurement. Instead, it is recommended that a given telemetry point be requested at least twice (with at least 150 ms of time between requests) to rule out an erroneous ADC reading.

10 FAULT PROTECTION

The EPS card has a number of internal hardware and software-based fault protection features designed to minimize the potential of damage to the EPS card as well as the rest of the spacecraft due to anomalous events. These protections include:

- Power converter overcurrent protection
- Switch 1-4 overcurrent protection
- Switched output protection from battery bus abnormal voltage transient events
- EPS internal watchdog timer
- Battery overcurrent, undercurrent, and overvoltage protection

10.1 Power Converter Overcurrent Protection

The BCR, 3.3-Volt, 5-Volt, and 12-Volt power converters have pulse-by-pulse current limits that cause the converters to fold-back if the maximum output current is exceeded. These limits are detailed in Section 5.4.2. In this mode, the output voltage will sag until the load current decreases to the current limit.

10.2 Battery Overvoltage / Overcharge Current Protection

The EPS card has a hardware protection circuit that commands a high-side series switch to open if either the battery voltage exceeds the overvoltage threshold or if the charge current exceeds the overcurrent-charge threshold. This circuit has significant hysteresis for the overcurrent mode which will keep it off for ~0.5 seconds before it is closed. If it is tripped due to overvoltage, the switch will not be closed until the battery voltage sensed on the EPS card drops below the falling overvoltage threshold. The overvoltage protection also causes the hysteresis on the overcharge current protection to be activated, which may cause a delay of up to several seconds if the charge current was above 2 A.

The EPS battery voltage telemetry is sensed on the battery side of this circuit and is independent of the overvoltage protection circuit.

There is a bypass diode in parallel with the overvoltage/overcharge current protection circuit that allows the battery to be discharged when the fault protection is active.

10.2.1 Battery Bus Abnormal Transient Voltage Protection

If the battery overvoltage protection switch is opened, the battery bus will experience an overvoltage condition in which the output voltage of the power converter is limited by an overvoltage clamp to approximately 21V. The microcontroller will command the switched battery bus outputs open if this condition is detected to protect both the switched outputs as well as ensure that the switches are not operated with their gate-source voltage not fully saturated.

When this fault is detected, the battery protection fault error flag will be set in the system error byte. This flag must be cleared before switched battery power outputs can be commanded closed via the CC&DH interface. Attempts to clear this flag while the fault exists will be rejected and an “Illegal Command” response will be returned to the flight computer. See Section 12.5 for additional information regarding the battery protection fault error flag.

When the fault exists, commands to close any switched battery power outputs will be rejected and an “Illegal Command” response will be returned to the flight computer.

When the fault is cleared, the altered switched outputs will remain open but can be commanded closed again.

10.3 Battery Undervoltage / Overdischarge Current Protection

The EPS contains a hardware protection circuit for preventing the battery from being discharged if it either enters a low state of charge or if the discharge current exceeds a hardware limit. If either of these events occurs, a low-side switch will be opened. With this low-side switch open, the only loads on the battery will be the battery protection circuit. The EPS will continue to function in this mode if solar array power is available. If there is no solar array power available, then the EPS card will be in an inactive state until either the battery exits the undervoltage or overdischarge current state or solar array power is available.

This circuit has significant hysteresis to ensure that an overcurrent trip will not be recycled quickly (since that can cause thermal stress/failure to the low-side protection switch that is being toggled). Typical reset rates for the overcurrent protection are 0.5 seconds and depend on the peak current as well as the duration of the peak.

The undervoltage and overdischarge current circuits will activate each other’s hysteresis. That means that an overdischarge current event at a battery voltage below the undervoltage rising threshold will cause the undervoltage protection to be active until the battery voltage exceeds the rising threshold. A short undervoltage transient may also cause the overcurrent circuit hysteresis to be active, which can have the aforementioned several second reset time.

When the falling threshold for undervoltage is met, the EPS will shed all switched loads and disable the 5-Volt converter. The MCU will also default all configuration and control registers.

During the existence of this fault, commands to close any switched output will be rejected and an “Illegal Command” response will be returned to the flight computer.

When the system enters undervoltage, the undervoltage fault error flag will be set in the system error register. This flag must be cleared before switched outputs can be commanded on via the CC&DH interface. Attempts to clear this flag while the fault exists will be rejected and an “Illegal Command” response will be returned to the flight computer. See Section 12.5 for additional information regarding the undervoltage error flag.

Once the rising threshold is met, the 5-Volt converter will be re-enabled but the switched outputs will remain open. If a dedicated CC&DH switched output is configured, this switch will be commanded on as part of the undervoltage exit routine.

During system start-up, if the rising threshold for battery undervoltage is not met, the EPS will not enable the 5-Volt converter nor close the dedicated CC&DH switched output (if applicable). Identical to that above, the 5-Volt converter will be enabled once the rising threshold is met and the dedicated CC&DH switched output will be closed (if applicable).

10.4 Internal Watchdog Timer

The EPS card has an internal watchdog timer which power cycles the microcontroller if the microcontroller enters a state in which it stops resetting the timer. This power cycle will cause all microcontroller-controlled functions to be reset into their default power-on configuration.

Note: This watchdog timer is not the spacecraft watchdog timer which is configurable via the CC&DH interface.

See Section 5.4.8 for the relevant specification of the EPS's watchdog timer.

10.5 Switch 1-4 Overcurrent Protection

The protection on switches 1-4 will activate when the programmed limit is exceeded. This protection does not limit the switched current of the output. Instead it severs power to the load in event of an overcurrent fault.

In the case of the 3.3-Volt, 5-Volt, and 12-Volt outputs, the current may generally be bounded by the switch source. The switches themselves are rated for 45A; that said, they are not thermally capable of sustaining that current for any significant amount of time.

The peak currents may exceed the converter fold-back limits for short periods due to discharging output capacitance. The switches supplying battery power do not have a fold-back because the battery can supply current into them. For these switches, the peak current is generally limited by either the ESR of the battery and the ohmic resistance of the path through the switch or by the internal cell protection of the battery (assuming the battery cells have active/passive protection).

See Section 8.6 for additional information on switch overcurrent protection operation.

10.6 Battery Over-Temperature Protection

The EPS does not report battery over-temperature flags, nor does it act on a battery over-temperature fault. The flight computer is solely responsible for checking and maintaining battery temperature(s).

10.7 External Watchdog Timer

The EPS accepts an external watchdog timer input over the serial CC&DH interface. There are two reset modes, configurable via the following register:

0x15 – External Watchdog Reset Mode Register

The default reset mode is a Global Reset. In this mode, when a timeout occurs, all spacecraft subsystems, including the EPS, will be powered off. Specifically, the EPS will stop petting its own watchdog timer, resulting in a power cycle of the MCU. After the EPS watchdog timer re-energizes the MCU, the EPS will follow the standard start-up sequence as described in Section 6.3.1. Due to the nature of this mode, all configurable EPS parameters will be defaulted upon MCU restart.

Via a write to the EWRMR, the reset mode can be set to a Non-Global Reset. In this mode, when a timeout occurs, all spacecraft subsystems, except the EPS itself, will be powered off. After a

set hold-off time, the EPS will re-enable all converters and re-energize the CC&DH switched output (if applicable). As part of this sequence the EPS will default all configurable parameters such that its state is equivalent to that of initial spacecraft deployment.

The following registers are relevant to the configuration and control of the external watchdog timer:

- *0x14 - External Watchdog Configuration Register*
  - This register contains both the enable/disable bit and the 7-bit timeout duration for the timer.
  - See Section 12.6.2.5 for details on register utilization.
- *0x15 – External Watchdog Reset Mode Register*
  - This register specifies the external watchdog reset mode to be executed upon a watchdog timeout.
  - See Section 12.6.2.6 for details on register utilization.
- *0x30 - External Watchdog Control Register*
  - This register handles external watchdog timer petting.
  - See Section 12.6.3.1 for details on register utilization.

All external watchdog functionality is overridden by the GSE-only, active-low hardware signal *I2C_WD_DIS_N.*

10.7.1 Non-Global External Watchdog Timeout

When the reset mode is configured as a Non-Global Reset via the EWRMR, the CC&DH watchdog timer is enabled via the EWCFR, and the timer is not pet via the EWCTR within the configured duration, the EPS watchdog will execute a non-global spacecraft reset. This reset operates as follows:

1. Open all switched outputs
2. Sequence down all power converters
3. Restore all EPS configurable parameters to default states
4. Pause for a finite hold-off time (t_{HO})
5. Sequence up all power converters
6. Re-energize the CC&DH switched output (If applicable).

Note: If a system fault exists during the re-initialization of the system, this reset sequence may not exactly follow the depiction in Figure 7, depending on the fault. See Section 10 for details on how individual faults affect system initialization. If a converter is not enabled, due to the existence of a fault, the respective delay is not be asserted.

The following figure depicts the non-global spacecraft reset sequence.

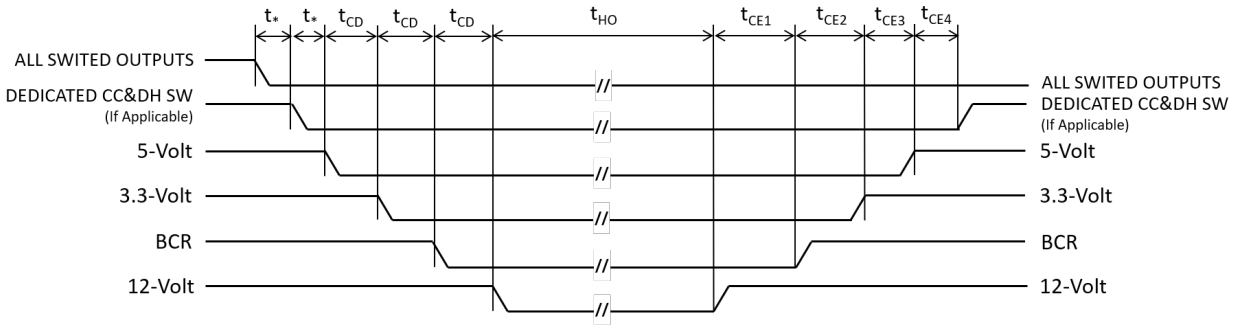


Figure 7. External Watchdog Non-Global Reset Sequence

Table 22. External Watchdog Non-Global Reset Timing Parameters

Symbol	Parameter	Condition	Min	Nom	Max	Units
t_*	Non-Tightly Controlled Timing (Note 1)	–	–	–	–	–
t_{CD}	Converter Disable Command Sequence Interval	–	–	5	–	ms
t_{CE1}	Converter Enable Command Sequence Interval, 12-Volt	–	–	25	–	ms
t_{CE2}	Converter Enable Command Sequence Interval, BCR	–	–	185	–	ms
t_{CE3}	Converter Enable Command Sequence Interval, 5-Volt	–	–	90	–	ms
t_{CE4}	Converter Enable Command Sequence Interval, 3.3-Volt	–	–	20	–	ms
t_{HO}	System Hold-Off Period	–	–	1000	–	ms

1. Sequencing is guaranteed as depicted but timing is not tightly controlled. The total duration is anticipated to be largely under 1ms.

After the watchdog reset sequence concludes, the EPS will be in its default configuration. This configuration is equivalent to the state that the EPS is in after the spacecraft is initially deployed and the separation switches are opened.

10.7.2 Global External Watchdog Timeout

When the reset mode is configured as a Global Reset via the EWRMR, the CC&DH watchdog timer is enabled via the EWCFR, and the timer is not pet via the EWCTR within the configured duration, the EPS watchdog will execute a global spacecraft reset. This reset operates as follows:

1. Open all switched outputs
2. Sequence down all power converters
3. Stop petting internal watchdog timer
4. Wait for internal watchdog induced power cycle
5. Start-up per standard start up sequence (Section 6.3.1)

Note: If a system fault exists during the re-initialization of the system, this reset sequence may not exactly follow the depiction in Figure 7, depending on the fault. See Section 10 for details on

how individual faults affect system initialization. If a converter is not enabled, due to the existence of a fault, the respective delay is not be asserted.

The following figure depicts the global spacecraft reset down sequence. The EPS follows the start-up sequence defined in Section 6.3 after the 3.3V housekeeping rail (3.3Vhk) is back in regulation.

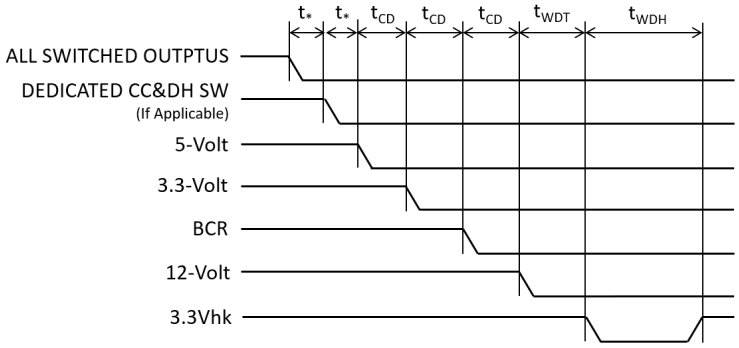


Figure 8. External Watchdog Global Reset Sequence

Table 23. External Watchdog Global Reset Timing Parameters

Symbol	Parameter	Condition	Min	Nom	Max	Units
t_*	Non-Tightly Controlled Timing (Note 1)	–	–	–	–	–
t_{CD}	Converter Disable Command Sequence Interval	–	–	5	–	ms
t_{WDT}	Internal Watchdog Timeout Duration	–	See Table 12			–
t_{WDH}	Internal Watchdog Hold-Off Duration	–				–

1. Sequencing is guaranteed as depicted but timing is not tightly controlled. The total duration is anticipated to be largely under 1ms.

After the watchdog reset sequence concludes, the EPS will be in its default configuration. This configuration is equivalent to the state that the EPS is in after the spacecraft is initially deployed and the separation switches are opened.

10.8 Fault Reporting

The EPS's error registers are described in Section 12.6.6.

10.9 Event Counters

The EPS has several event counters that are stored in non-volatile memory that count the number of times certain faults have occurred. These counters are 8-bit numbers and will roll-over once they exceed 255. These system status register counters are detailed in Section 12.6.5

11 ELECTRICAL INTERFACES

11.1 J3 – Battery/Solar Array Connector

The EPS battery/solar array connector interfaces to the spacecraft battery assembly, solar array, and inhibit switches. The interface provides several pins for battery supply and return; Solar array power and return; 4 thermistor inputs and returns; 2 battery heater outputs and returns; and three inhibit interfaces. The connector shell is electrically connected to chassis ground.

Ref. Designator: J3
Connector Type: 51-Pin, Right Angle Through Hole, 3-Row, Micro-D, Female
Part Number: GMR7590-51S1BSU
Manufacturer: Glenair, Inc.
Pin Definition:

Pin	Signal	Description	Pin	Signal	Description
1	SA_NEG	Spacecraft Solar Array Return	27	GND	Electrical Ground
2	SA_NEG	Spacecraft Solar Array Return	28	THERMISTOR_2	Thermistor positive (Note 1)
3	SA_NEG	Spacecraft Solar Array Return	29	THERMISTOR_4	Thermistor positive (Note 1)
4	SA_NEG	Spacecraft Solar Array Return	30	BATT_POS	Spacecraft Battery Supply
5	INHIBIT_2_P2	Inhibit 2	31	BATT_NEG	Spacecraft Battery Return
6	INHIBIT_2_P1	Inhibit 2	32	BATT_NEG	Spacecraft Battery Return
7	INHIBIT_1_P2	Inhibit 1	33	BATT_POS	Spacecraft Battery Supply
8	INHIBIT_1_P1	Inhibit 1	34	BATT_POS	Spacecraft Battery Supply
9	GND	Electrical Ground	35	BATT_NEG	Spacecraft Battery Return
10	GND	Electrical Ground	36	SA_POS	Spacecraft Solar Array Positive
11	THERMISTOR_3	Thermistor positive (Note 1)	37	SA_POS	Spacecraft Solar Array Positive
12	BATT_NEG	Spacecraft Battery Return	38	SA_POS	Spacecraft Solar Array Positive
13	BATT_NEG	Spacecraft Battery Return	39	SA_POS	Spacecraft Solar Array Positive
14	BATT_NEG	Spacecraft Battery Return	40	HEATER_1	Battery Heater 1 Output
15	BATT_NEG	Spacecraft Battery Return	41	HEATER_2	Battery Heater 2 Output
16	BATT_NEG	Spacecraft Battery Return	42	GND	Electrical Ground
17	BATT_NEG	Spacecraft Battery Return	43	GND	Electrical Ground
18	BATT_NEG	Spacecraft Battery Return	44	THERMISTOR_1	Thermistor positive (Note 1)
19	SA_NEG	Spacecraft Solar Array Return	45	BATT_POS	Spacecraft Battery Supply
20	SA_POS	Spacecraft Solar Array Positive	46	BATT_POS	Spacecraft Battery Supply
21	SA_POS	Spacecraft Solar Array Positive	47	BATT_POS	Spacecraft Battery Supply
22	SA_NEG	Spacecraft Solar Array Return	48	BATT_POS	Spacecraft Battery Supply
23	INHIBIT_3_P2	Inhibit 3	49	BATT_POS	Spacecraft Battery Supply

Pin	Signal	Description	Pin	Signal	Description
24	INHIBIT_3_P1	Inhibit 3	50	BATT_POS	Spacecraft Battery Supply
25	GND	Electrical Ground	51	BATT_POS	Spacecraft Battery Supply
26	GND	Electrical Ground			

1. Thermistor inputs are each pulled up to 2.50V via 4.99K 0.01% resistor

11.2 J2 – Switched Output and Serial I/F Connector

The switched and unswitched power interfaces to the spacecraft along with serial interfaces are on the J2 connector. The interface provides 8 switched power outputs with returns; an I2C serial interface; an external reset command, a SPI serial interface; and unswitched power for each of the externally available power supplies. The connector shell is electrically connected to chassis ground.

Ref. Designator: J2
Connector Type: 51-Pin, Right Angle Through Hole, 3-Row, Micro-D, Male
Part Number: GMR7590-51P1BSU
Manufacturer: Glenair, Inc.
Pin Definition:

Pin	Signal	Description	Pin	Signal	Description
1	SW8_OUT	Switch Output 8	27	GND	Electrical Ground
2	12V_OUT	Unswitched 12V	28	GND	Electrical Ground
3	VBATT_OUT	Unswitched Battery Bus	29	SPI_MOSI	SPI
4	5V_OUT	Unswitched 5V	30	SPI_SCK	SPI
5	GND	Electrical Ground	31	I2C_SCL	I2C
6	RESET_N	EPS External Reset	32	SW2_OUT	Switched Output 2
7	GND	Electrical Ground	33	SW1_OUT	Switched Output 1
8	GND	Electrical Ground	34	SW1_OUT	Switched Output 1
9	GND	Electrical Ground	35	GND	Electrical Ground
10	GND	Electrical Ground	36	VBATT_OUT	Unswitched Battery Bus
11	GND	Electrical Ground	37	VBATT_OUT	Unswitched Battery Bus
12	GND	Electrical Ground	38	SW7_OUT	Switch Output 7
13	SPI_MISO	SPI	39	SPI_SS	SPI
14	I2C_SDA	I2C	40	SW3_OUT	Switch Output 3
15	GND	Electrical Ground	41	SW5_OUT	Switch Output 5
16	GND	Electrical Ground	42	SW4_OUT	Switch Output 4
17	GND	Electrical Ground	43	SW4_OUT	Switch Output 4
18	GND	Electrical Ground	44	GND	S/A String Input
19	VBATT_OUT	Unswitched Battery Bus	45	GND	S/A Return
20	VBATT_OUT	Unswitched Battery Bus	46	SW6_OUT	Switch Output 6

Pin	Signal	Description	Pin	Signal	Description
21	VBATT_OUT	Unswitched Battery Bus	47	3V3_OUT	Unswitched 3.3V
22	GND	Electrical Ground	48	SW2_OUT	Switch Output 2
23	GND	Electrical Ground	49	SW2_OUT	Switch Output 2
24	SW3_OUT	Switched Output 3	50	SW1_OUT	Switch Output 1
25	GND	Electrical Ground	51	SW1_OUT	Switch Output 1
26	GND	Electrical Ground			

1. Thermistor inputs are each pulled up to 2.50V via 4.99K 0.01% resistor

11.3 J1 - Ground Support Equipment (GSE) Connector

The EPS GSE connector interfaces to the spacecraft CC&DH interface, the system programming interface (for manufacturer use only), and several system signals including all 3 inhibits (separation switches), the I2C watchdog disable, and the system level reset command.

Ref. Designator: J1
Connector Type: 22-Pin, Horizontal Surface Mount, 2-Row, Nano-Strip
Part Number: PZN-22-AA
Manufacturer: Omnetics Corporation
Pin Definition:

Pin	Signal	Description	Pin	Signal	Description
1	NC (12V_HK_Test)	Manufacturer Use Only	12	INHIBIT_1_P1	Inhibit 1
2	INHIBIT_3_P2	Inhibit 3	13	GND	Electrical Ground
3	NC (30V_HK_Test)	Manufacturer Use Only	14	GND	Electrical Ground
4	INHIBIT_3_P1	Inhibit 3	15	SPI_SCK	CC&DH SPI Clock
5	NC (3.3V_HK_Test)	Manufacturer Use Only	16	I2C_SPI_WD_DIS_N	CC&DH I2C Data Signal
6	INHIBIT_1_P2	Inhibit 1	17	SPI_MISO	CC&DH SPI Master In Slave Out
7	RESET_N	Active Low Spacecraft Watchdog Disable	18	NC (MCU_INT_RESET_N)	Manufacturer Use Only
8	INHIBIT_2_P2	Inhibit 2	19	I2C_SDA	CC&DH I2C Data
9	SPI_SS	CC&DH SPI Slave Select	20	NC (PROG_MISO)	Manufacturer Use Only
10	INHIBIT_2_P1	Inhibit 2	21	I2C_SCL	CC&DH I2C Clock
11	SPI_MOSI	CC&DH SPI Master Out Slave In	22	NC (PROG_MOSI)	Manufacturer Use Only

12 COMMAND, CONTROL, AND DATA HANDLING INTERFACE

12.1 Overview

The EPS provides two serial interfaces for all system configuration, control, and telemetry read-out. The first CC&DH interface is a 3.3V Inter-Integrated Circuit (I^2C) interface. The EPS operates as a slave on an I2C bus, responding to the 7-bit address specified in Section 12.2.4. The second CC&DH interface is a 3.3V Serial Peripheral Interface (SPI). The EPS operates as a slave on a SPI bus as well.

The EPS is controlled through writes and reads to the various system registers via I2C or SPI. Each of these registers is described in detail in Section 12.6. Section 12.2.6 and Section 12.3.5 describe the expected write and read command structures for both I2C and SPI, respectively.

12.2 Inter-Integrated Circuit (I2C) Interface

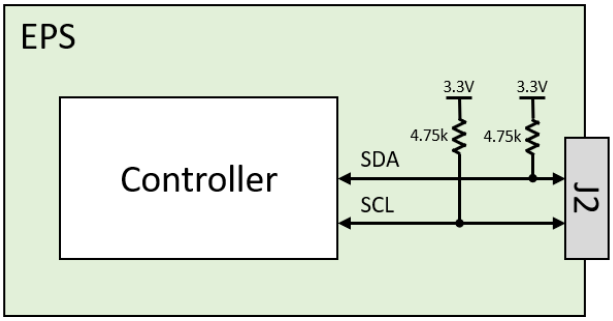


Figure 9. I^2C Electrical Block Diagram

12.2.1 Electrical Parameters

Table 24. I^2C Interface Electrical Parameters

Symbol	Parameter	Condition	Min	Nom	Max	Units
V_{BUS}	I^2C Bus Voltage		3.0	3.3	3.6	V
R_{PU}	SDA/SCL Pull-Up Resistors **(Note 1)**	f_{SCL} <= 100KHz	1k	4.75k	8k	Ω
		f_{SCL} > 100KHz			2.4k	Ω
f_{SCL}	SCL Clock Frequency		-	-	400	kHz
V_{IL}	Input Low Voltage		-0.5	-	0.3 * V_{BUS}	V
V_{IH}	Input High Voltage		0.7 * V_{BUS}	-	V_{BUS} + 0.5	V
V_{HYS}	Hysteresis of Schmitt Trigger Inputs		0.05 * V_{BUS}	-	-	V
V_{OL}	Output Low Voltage		0	-	0.4	V

1. Pull-up resistance is the equivalent resistance of all pull-up resistors on a given line, across all devices on a bus. Having an equivalent resistance of less than the specified minimum may overstress the MCU I/O.

12.2.2 Additional Bus Pull-Ups

EPS I2C and SPI bus pull-up resistors should be limited to a minimum equivalent parallel resistance of 500 Ohms. Having lower resistance than this may prevent the EPS card from

being able to power cycle the internal 3.3V housekeeping voltage during the MCU watchdog reset which will disable the EPS watchdog reset functionality.

12.2.3 Timing Diagram

Figure 10. EPS I²C Timing Diagram

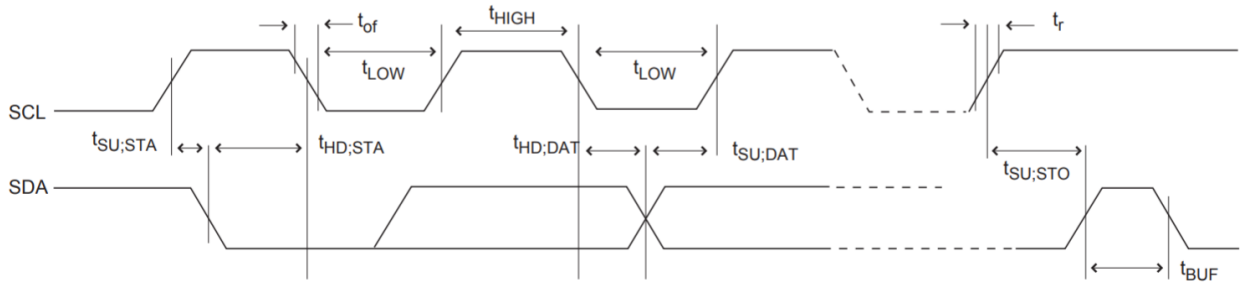


Table 25. I²C Interface Timing Parameters

Symbol	Parameter	Condition	Min	Max	Units
$t_{HD;STA}$	Hold Time (repeated) START Condition	f_{SCL} ≤ 100kHz	4.0	–	µs
		f_{SCL} > 100kHz	0.6	–	µs
t_{LOW}	Low Period of the SCL Clock	f_{SCL} ≤ 100kHz	4.7	–	µs
		f_{SCL} > 100kHz	1.3	–	µs
t_{HIGH}	High period of the SCL Clock	f_{SCL} ≤ 100kHz	4.0	–	µs
		f_{SCL} > 100kHz	0.6	–	µs
$t_{SU;STA}$	Setup Time for a Repeated START Condition	f_{SCL} ≤ 100kHz	4.7	–	µs
		f_{SCL} > 100kHz	0.6	–	µs
$t_{HD;DAT}$	Data Hold Time	f_{SCL} ≤ 100kHz	0	3.45	µs
		f_{SCL} > 100kHz	0	0.9	µs
$t_{SU;DAT}$	Data Setup Time	f_{SCL} ≤ 100kHz	250	–	ns
		f_{SCL} > 100kHz	100	–	ns
$t_{SU;STO}$	Setup Time for STOP Condition	f_{SCL} ≤ 100kHz	4.0	–	µs
		f_{SCL} > 100kHz	0.6	–	µs
t_{BUF}	Bus Free Time Between a STOP and START Condition	f_{SCL} ≤ 100kHz	4.7	–	µs

12.2.4 Slave Address

The EPS only operates as a slave on an I²C bus and exclusively acknowledges commands addressed to the 7-bit address of **0x2B**.

12.2.5 General Call Address

The EPS will not recognize the general call address and therefore will not acknowledge the address nor the subsequent data byte(s). The EPS will only respond to commands outlined in this document and addressed to the 7-bit address listed Section 12.2.4.

12.2.6 Transaction Structure

I2C transactions with the EPS shall follow the structure depicted in Figure 11 below. The transaction is initiated via a master-asserted start condition followed by the 7-bit EPS slave

address and write bit (0). Upon successful reception, the EPS will respond with an ACK, signifying that it is ready to receive the next byte in the sequence. The master shall then send the command parameters: a single read/write bit concatenated with a 7-bit register address, the data byte, and the corresponding CRC byte. Each of these bytes will be ACK'd by the EPS upon successful reception. The master shall then send a repeat start condition followed by the 7-bit EPS slave address and read bit (1). Upon successful reception, the EPS will respond with an ACK and then send 27 bytes. The EPS expects that the master ACK each byte after it is sent via the master-driven clock with the exception of the last byte which shall be NACK'd. Following this NACK, the master shall terminate the transaction by asserted the stop condition.

Sections 12.2.6.1, 12.2.6.2, and 12.2.6.3 below describe the specific structure of a read, write, and telemetry request, respectively. Each section also details how data is decoded from the 27-byte response.

At any point, if the master does not comply with this command structure, or takes longer than the specified timeout period, the EPS will abort the transaction and return to normal operation. The system will then respond to the next valid request. See Section 12.2.7 for additional details on transaction timeout.

	SLAVE ADDRESS							R/$\overline{W}$		R/$\overline{W}$	ADDRESS BYTE							
S	S6	S5	S4	S3	S2	S1	S0	0	A	1/0	A6	A6	A4	A3	A2	A1	A0	A

DATA BYTE									CRC BYTE								
D7	D6	D5	D4	D3	D2	D1	D0	A	C7	C6	C6	C4	C3	C2	C1	C0	A

	SLAVE ADDRESS							R/$\overline{W}$		DATA BYTE 15								
RS	S6	S5	S4	S3	S2	S1	S0	1	A	D7	D6	D6	D4	D3	D2	D1	D0	A

DATA BYTE 14									CRC BYTE 8									
D7	D6	D6	D4	D3	D2	D1	D0	A	C7	C6	C6	C4	C3	C2	C1	C0	A	...

DATA BYTE 1									DATA BYTE 0								
D7	D6	D6	D4	D3	D2	D1	D0	A	D7	D6	D6	D4	D3	D2	D1	D0	A

CRC BYTE 1									ERROR BYTE 1								
C7	C6	C6	C4	C3	C2	C1	C0	A	E7	E6	E6	E4	E3	E2	E1	E0	A

ERROR BYTE 0									CRC BYTE 0									
E7	E6	E6	E4	E3	E2	E1	E0	A	C7	C6	C6	C4	C3	C2	C1	C0	$\overline{A}$	P

MASTER DRIVEN
SLAVE DRIVEN
A: ACKNOWLEDGE (SDA LINE LOW)

$\overline{A}$: NOT ACKNOWLEDGE (SDA LINE HIGH)
S: START CONDITION
RS: REPEAT START CONDITION
P: STOP CONDITION

Figure 11. I2C Transaction Transmission Diagram

As seen in the transmission diagram above, the I2C interface employs CRCs to ensure interface robustness. Section 12.4 details the CRC scheme used throughout an I2C transaction.

12.2.6.1 Master Register Write Command

An 8-bit EPS register is modified via a Master Register Write Command. The first 4 bytes of the I2C command shall be structured as follows:

	SLAVE ADDRESS							R/$\overline{W}$		R/$\overline{W}$	ADDRESS BYTE							
S	S6	S5	S4	S3	S2	S1	S0	0	A	0	A6	A6	A4	A3	A2	A1	A0	A

DATA BYTE									CRC BYTE								
D7	D6	D5	D4	D3	D2	D1	D0	A	C7	C6	C6	C4	C3	C2	C1	C0	A

Figure 12. I2C Master Register Write Command Byte Structure

Upon reception of a valid write bit (R/$\overline{W}$ = 0), register address, and data byte, validated via the respective CRC byte, the data byte is written to the specified address and the system is updated accordingly. If the data is invalid, the data byte is not written to the specified address and the system remains unchanged. Reasons for rejected write commands include an invalid register address, illegal register value, illegal operation, or invalid CRC.

Whether accepted or rejected, the EPS will always respond to a write command with the standard 27-byte response. A proper response will be structured as follows:

BYTE INDEX	BYTE NAME	BYTE MAPPING
26-3	-	RESERVED
2	ERROR BYTE 1	ERROR BYTE 1
1	ERROR BYTE 0	ERROR BYTE 0
0	CRC BYTE 0	CRC BYTE 0

Following the repeat start condition are 24 reserved bytes followed by the two error bytes and their corresponding CRC byte.

An error bit sequence of all 0s implies that the command was executed successfully and that there are no command nor system-level errors to report. Section 12.5 outlines the error flags associated with each error bit.

Note: Not all registers are writeable. If a master attempts to write to a read-only address, the command will be ignored, and the appropriate error bit will be set in the response.

12.2.6.2 Master Register Read Command

An 8-bit EPS register is read via a Master Register Read Command. The first four bytes of the I2C command shall be structures as follows:

	SLAVE ADDRESS							R/$\overline{W}$		R/$\overline{W}$	ADDRESS BYTE							
S	S6	S5	S4	S3	S2	S1	S0	0	A	1	A6	A6	A4	A3	A2	A1	A0	A

RESERVED									CRC BYTE								
0	0	0	0	0	0	0	0	A	C7	C6	C6	C4	C3	C2	C1	C0	A

Figure 13. I2C Master Register Read Command Byte Structure

Upon reception of a valid read bit (R/$\overline{W}$ = 1) and register address (and reserved byte), validated via the respective CRC byte, the value of the specified register will be transmitted on the bus as part of the standard 27-byte response. If the command is invalid, the EPS will respond with the appropriate error flag. Reasons for rejected read commands include an invalid register address or CRC.

A proper response will be structured as follows:

BYTE INDEX	BYTE NAME	BYTE MAPPING
26	DATA BYTE 15	RESERVED (0x00)
25	DATA BYTE 14	DATA BYTE
24	CRC BYTE 8	CRC BYTE 8
23-3	-	RESERVED
2	ERROR BYTE 1	ERROR BYTE 1
1	ERROR BYTE 0	ERROR BYTE 0
0	CRC BYTE 0	CRC BYTE 0

Following the repeat start condition is a reserved byte, the requested data byte, and then the corresponding CRC byte. Note that CRC BYTE 8 pertains to both the preceding reserved byte and data byte. Following CRC BYTE 8 are the two error bytes and their corresponding CRC byte.

An error bit sequence of all 0s implies that the command was executed successfully and that there are no command nor system-level errors to report. Section 12.5 outlines the error flags associated with each error bit.

12.2.6.3 Master Telemetry Bank Read Command

An 8-measurement telemetry bank is read via a Master Telemetry Bank Read Command. The first 4 bytes of the I2C command shall be structures as follows:

	SLAVE ADDRESS							R/$\overline{W}$		R/$\overline{W}$	ADDRESS BYTE							
S	S6	S5	S4	S3	S2	S1	S0	0	A	1	A6	A6	A4	A3	A2	A1	A0	A

RESERVED									CRC BYTE								
0	0	0	0	0	0	0	0	A	C7	C6	C6	C4	C3	C2	C1	C0	A

Figure 14. I2C Master Telemetry Bank Read Command Byte Structure

Upon reception of a valid read bit (R/$\overline{W}$ = 1) and register address (and reserved byte), validated via the respective CRC byte, the eight 10-bit telemetry measurements of the specified bank will be transmitted on the bus as part of the standard 27-byte response. If the command is invalid, the EPS will respond with the appropriate error flag. Reasons for rejected telemetry requests include an invalid register address or CRC.

A proper response will be structured as follows:

BYTE INDEX	BYTE NAME	BYTE MAPPING
26-25	DATA BYTE [15:14]	TELEMETRY POINT 7
24	CRC BYTE 8	CRC BYTE 8
23-22	DATA BYTE [13:12]	TELEMETRY POINT 6
21	CRC BYTE 7	CRC BYTE 7
20-19	DATA BYTE [11:10]	TELEMETRY POINT 5
18	CRC BYTE 6	CRC BYTE 6
17-16	DATA BYTE [9:8]	TELEMETRY POINT 4
15	CRC BYTE 5	CRC BYTE 5
14-13	DATA BYTE [7:6]	TELEMETRY POINT 3
12	CRC BYTE 4	CRC BYTE 4
11-10	DATA BYTE [5:4]	TELEMETRY POINT 2
9	CRC BYTE 3	CRC BYTE 3
8-7	DATA BYTE [3:2]	TELEMETRY POINT 1
6	CRC BYTE 2	CRC BYTE 2
5-4	DATA BYTE [1:0]	TELEMETRY POINT 0
3	CRC BYTE 1	CRC BYTE 1
2	ERROR BYTE 1	ERROR BYTE 1
1	ERROR BYTE 0	ERROR BYTE 0
0	CRC BYTE 0	CRC BYTE 0

Following the repeat start condition, eight telemetry points are transmitted as 3-byte sets. The first two bytes of the set consist of a 10-bit telemetry value with the most significant bits (MSBs) padded as zero. The third byte in the set is the corresponding CRC byte. Following the last telemetry point set are the two error bytes and their corresponding CRC byte.

An error bit sequence of all 0s implies that the command was executed successfully and that there are no command nor system-level errors to report. Section 12.5 outlines the error flags associated with each error bit.

12.2.7 Transaction Timeout

If the master, at any point during an I2C transaction, takes longer than 1 ms to perform the next required operation (ACK, NACK, clock, etc.), the EPS will abort the transaction and return to

normal operation. The system will then respond to the next valid request with the CC&DH Transaction Time-Out flag set in the system error byte.

12.3 Serial Peripheral Interface (SPI)

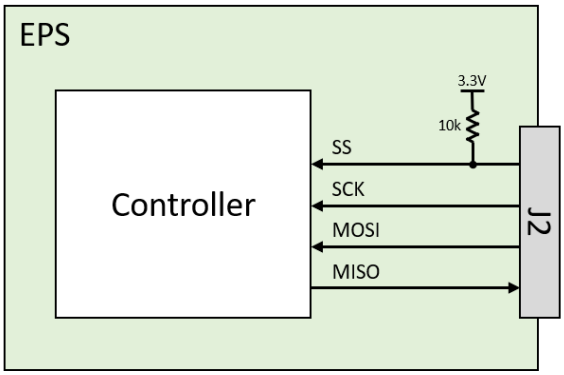


Figure 15. SPI Electrical Block Diagram

12.3.1 Electrical Parameters

Table 26. EPS SPI Interface Electrical Parameters

Symbol	Parameter	Condition	Min	Nom	Max	Units
V_{BUS}	SPI Bus Voltage		3.0	3.3	3.6	V
R_{PU}	On-Board Slave Select ($\overline{SS}$) Pull-Up Resistance		-	10.0	-	kΩ
f_{SCK}	SCK Clock Frequency **(See Section 12.3.5.5)**		-	1	-	MHz
V_{IL}	Input Low Voltage		-0.5	-	0.2 * V_{BUS}	V
V_{IH}	Input High Voltage		0.6 * V_{BUS}	-	V_{BUS} + 0.5	V
V_{OL}	Output Low Voltage		-	-	0.6	V
V_{OH}	Output High Voltage		2.2	-	-	V
I_{OL}	Output Sink Current		-	-	10.0	mA
I_{OH}	Output Source Current		-	-	10.0	mA

12.3.2 Additional Bus Pull-Ups

EPS I2C and SPI bus pull-up resistors should be limited to a minimum equivalent parallel resistance of 500 Ohms. Having lower resistance than this may prevent the EPS card from being able to power cycle the internal 3.3V housekeeping voltage during the MCU watchdog reset which will disable the EPS watchdog reset functionality.

12.3.3 Clock Polarity and Phase

The SPI interface of the EPS operates with the following clock polarity and phase.

Parameter	Leading Edge	Trailing Edge
Polarity	Rising	Falling
Phase	Sample	Setup

12.3.4 Timing Diagram

Figure 16. SPI Timing Diagram

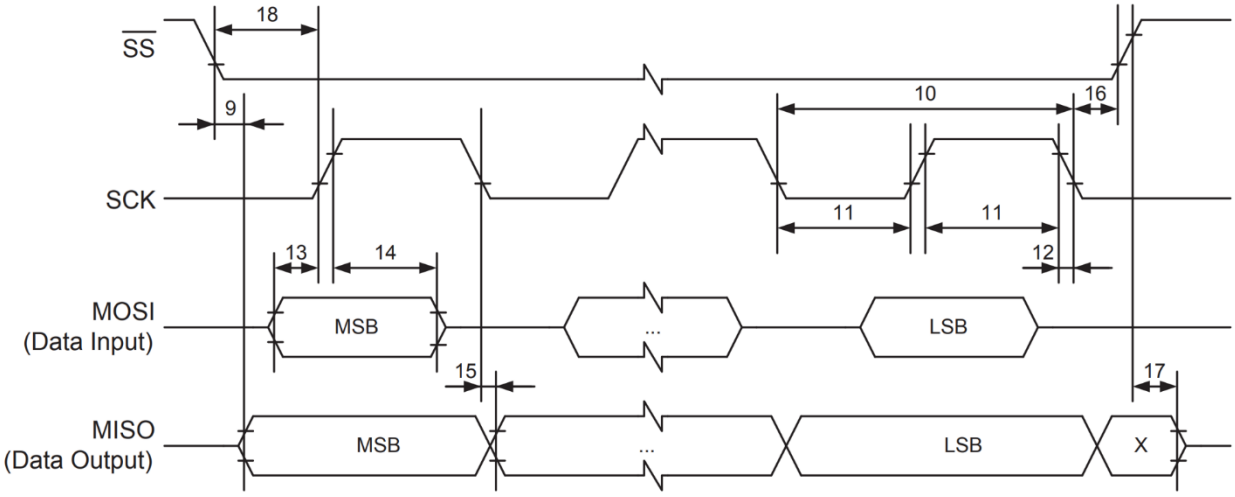


Table 27. SPI Interface Timing Parameters

ID	Parameter	Min	Nom	Max	Units
9	$\overline{SS}$ Low to Out	-	15	-	
10	SCK Period	1	-	-	us
11	SCK High/Low	500	-	-	ns
12	Rise/Fall Time	-	-	1.6	ns
13	Setup	10	-	-	ns
14	Hold	10	-	-	ns
15	SCK to Out	-	15	-	ns
16	SCK to $\overline{SS}$ High	20	-	-	ns
17	$\overline{SS}$ High to Tri-State	-	500	-	us
18	$\overline{SS}$ Low to SCK	250	-	-	ns

12.3.5 Polling Scheme

12.3.5.1 Overview

Given the absence of clock-stretching in the SPI protocol, a polling scheme has been implemented to prevent SPI transactions from altering the execution of time-sensitive software routines.

12.3.5.2 Command Sync Word

To initiate a SPI transaction, the master shall poll the EPS by repeatedly sending sequences of eight clock cycles until the command sync word is shifted into the master's data register. The EPS's command sync word is **0xB7**.

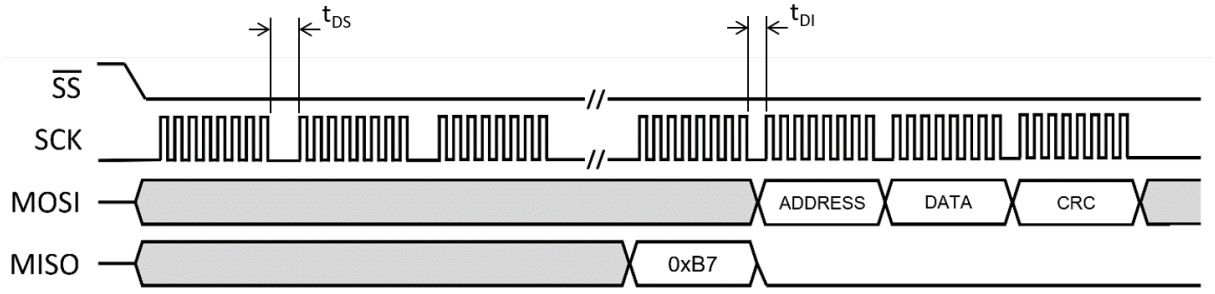


Figure 17. SPI Command Polling Timing Diagram

12.3.5.3 Response Sync Word

Given that the EPS takes varying amounts of time to process each command, the same polling scheme is implemented to synchronize the EPS's response. Upon successful transmission of the command parameters (address, data, and CRC bytes), the master shall poll the EPS by repeatedly sending sequences of eight clock cycles until the response sync word is shifted into the master's data register. After reception of the response sync word, the master shall clock the 27-byte response out of the EPS. The EPS's response sync word is **0x48**.

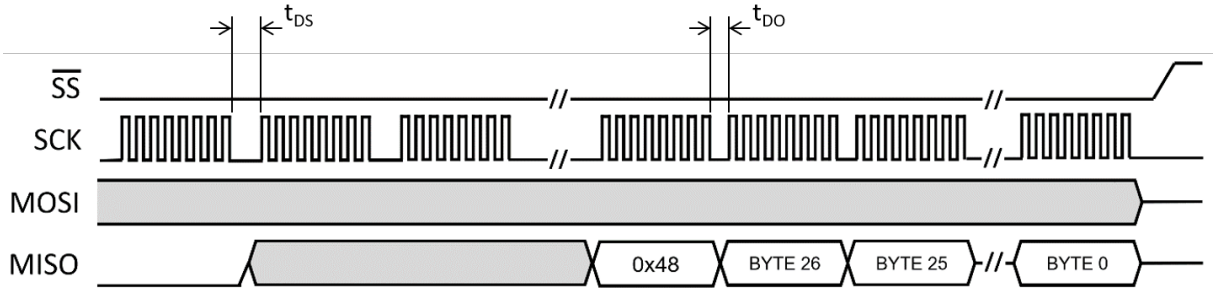


Figure 18. SPI Response Polling Timing Diagram

Note: The previous timing diagrams depict the expected polling behavior for both the command and response portions of a single, continuous SPI transaction. See Section 12.3.6 for the complete structure of the transaction beyond the required polling behavior.

12.3.5.4 Timing Specifications

The following timing specifications pertain to Figure 17 and Figure 18 above.

Table 28. SPI Inter-Byte Timing Parameters

Symbol	Parameter	Condition	Min	Nom	Max	Units
t_{DS}	Delay Between Sync Interrogations	–	–	25	–	us
t_{DI}	Delay Between Data In	–	3	4	–	us
t_{DO}	Delay Between Data Out	–	3	4	–	us

Note: Timing specifications may be bounded by transaction timeout parameters. See Section 12.3.5.5.

In the worst-case, the EPS may take up to 33 ms (a single 30 Hz period) to send a command sync word. Although, in practice, the duration is nominally 2 ms.

For the transmission of the response sync word, the worst-case duration is 8 ms (for timing-controlled switch commands). The typical duration is 1ms.

12.3.5.5 Timeout Specifications

The EPS implements a timeout on the SPI interface so as to guarantee performance during erroneous SPI transactions. The timeout on the SPI interface is on a byte-by-byte basis as depicted in the following figure.

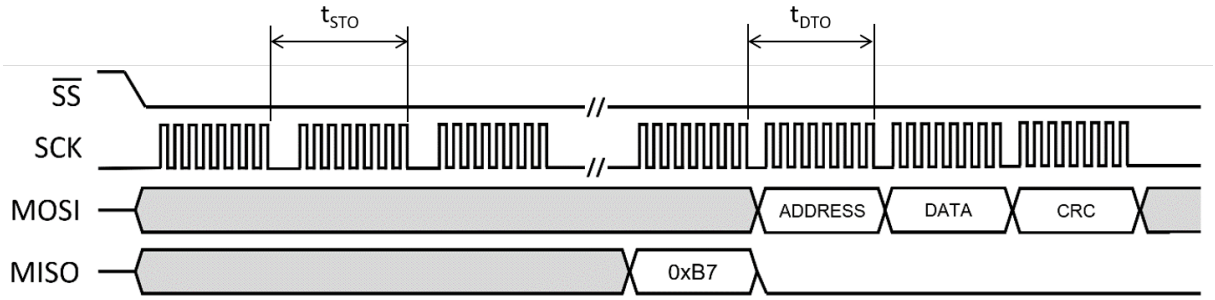


Figure 19. SPI Timeout Timing Diagram

Due to the differences in recommended (or required) delays between bytes (See Table 28), there are two timeout durations that the master must comply with in order to achieve a successful transaction. The first timeout window is for sync interrogations and is defined as the time shortly after the last bit of the proceeding interrogation word is clocked in to the SPI hardware up to the time that the last bit of the current interrogation word is clocked in to the SPI hardware (also defined as up to the time the last bit of the sync word is clocked out of the EPS SPI hardware).

The timeout window for data in and out is similarly defined. The timeout window for data in and out is defined as the time shortly after the last bit of the proceeding data word is clocked in to or out of the EPS SPI hardware up to the time that the last bit of the current data word is clocked in to or out of the SPI hardware.

Note: The above figure defines the timeout periods for a command sequence. The equivalent periods exist for the response sequence as well.

The table below provides the relevant timing parameters.

Table 29. SPI TImeout Timing Parameters

Symbol	Parameter	Condition	Min	Nom	Max	Units
t_{STO}	Single Interrogation Word Transmission Timeout	–	–	–	45	us
t_{DTO}	Single Data Word Transmission Timeout	–	–	–	12	us

Note: The recommended SCK frequency is 1 Mhz.

If at any point during a SPI transaction the timeout duration is exceeded, the EPS will abort the transaction and return to normal operation. After aborting the transaction, the system will respond to the next valid request with the CC&DH Transaction Time-Out flag set in the system error byte.

12.3.5.6 Example Transaction

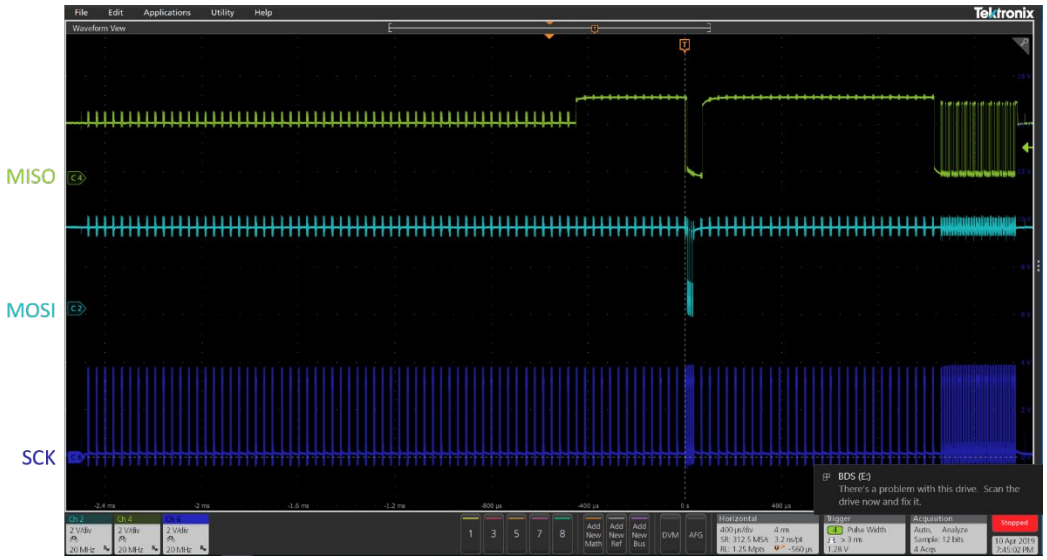


Figure 20. Example SPI Transaction with Polling Scheme

12.3.6 Transaction Structure

SPI transactions with the EPS shall follow the structure depicted in Figure 21 below. The transaction is initiated by the assertion of the active low Slave Select ($\overline{SS}$) signal. The master then polls the EPS as described in Section 12.3.5. Upon successful reception of the command sync word (0xB7), the master shall clock out the command parameters: a single read/write bit concatenated with a 7-bit register address, the data byte, and the corresponding CRC byte. The master shall then begin polling the EPS for a response as described in Section 12.3.5. When the EPS has completed all necessary operations and is ready to provide a response, it will respond to the polling with the response sync word (0x48). Upon reception of this byte, the master shall clock the 27-byte response out of the EPS. The transaction shall then be terminated by the release of the Slave Select signal.

Sections 12.3.6.1, 12.3.6.2, and 12.3.6.3 below describe the specific structure of a read, write, and telemetry request, respectively. Each section also details how data is decoded from the 27-byte response.

At any point, if the master does not comply with this command structure, or takes longer than the specified timeout period, the EPS will abort the transaction and return to normal operation.

The system will then respond to the next valid request. See Section 12.3.5.5 for additional details on transaction timeout.

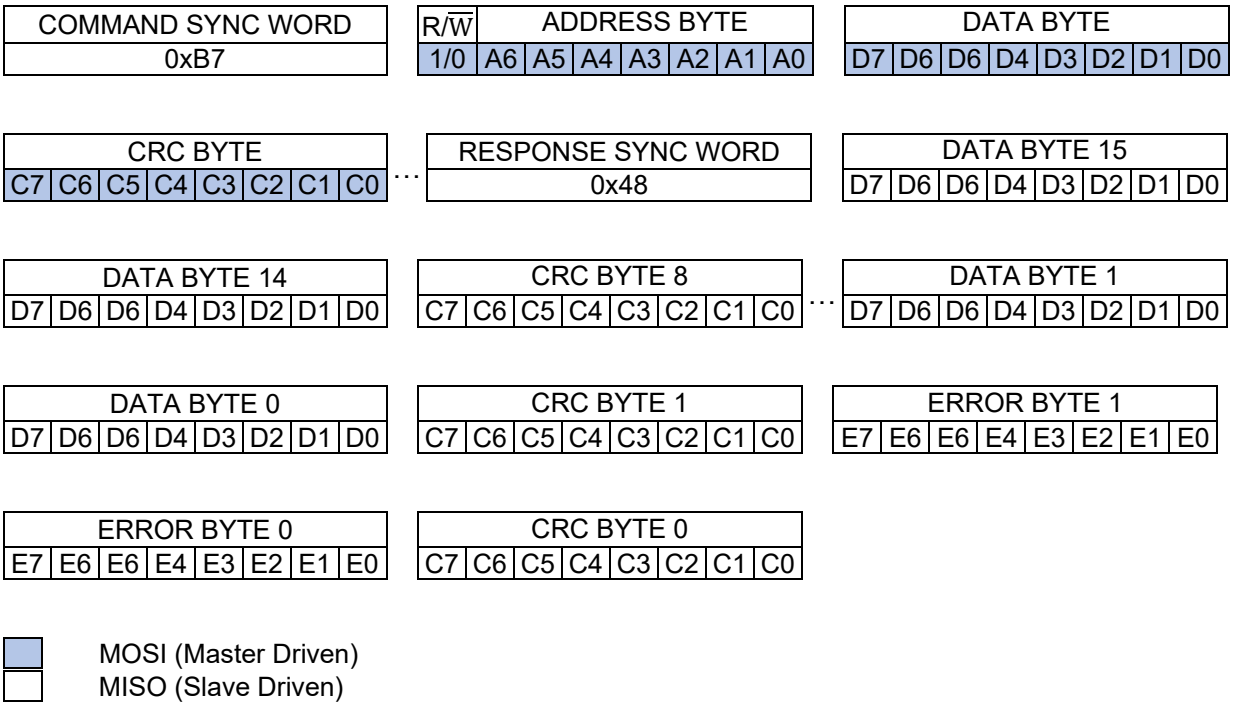


Figure 21. SPI Transaction Transmission Diagram

As seen in the transmission diagram above, the SPI interface employs CRCs to ensure interface robustness. Section 12.4 details the CRC scheme used throughout an SPI transaction.

12.3.6.1 Master Register Write Command

An 8-bit EPS register is modified via a Master Register Write Command. The first 4 bytes of the SPI command shall be structured as follows:

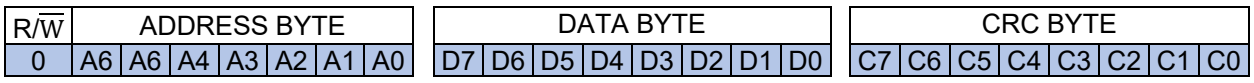


Figure 22. SPI Master Register Write Command Byte Structure

Upon reception of a valid write bit (R/$\overline{W}$ = 0), register address, and data byte, validated via the respective CRC byte, the data byte is written to the specified address and the system is updated accordingly. If the data is invalid, the data byte is not written the specified address and the system remains unchanged. Reasons for rejected write commands include an invalid register address, illegal register value, illegal operation, or invalid CRC.

Whether accepted or rejected, the EPS will always respond to a write command with the standard 27-byte response. A proper response will be structured as follows:

BYTE INDEX	BYTE NAME	BYTE MAPPING
26-3	-	RESERVED
2	ERROR BYTE 1	ERROR BYTE 1
1	ERROR BYTE 0	ERROR BYTE 0
0	CRC BYTE 0	CRC BYTE 0

Following the response sync word, 24 reserved bytes followed by the two error bytes and their corresponding CRC byte are transmitted by the EPS.

An error bit sequence of all 0s implies that the command was executed successfully and that there are no command nor system-level errors to report. Section 12.5 outlines the error flags associated with each error bit.

Note: Not all registers are writeable. If a master attempts to write to a read-only address, the command will be ignored, and the appropriate error bit will be set in the response.

12.3.6.2 Master Register Read Command

An 8-bit EPS register is read via a Master Register Read Command. The first four bytes of the SPI command shall be structures as follows:

R/$\overline{W}$	ADDRESS BYTE						
1	A6	A6	A4	A3	A2	A1	A0

RESERVED							
0	0	0	0	0	0	0	0

CRC BYTE							
C7	C6	C5	C4	C3	C2	C1	C0

Figure 23. SPI Master Register Read Command Byte Structure

Upon reception of a valid read bit (R/$\overline{W}$ = 1) and register address (and reserved byte), validated via the respective CRC byte, the value of the specified register will be transmitted on the bus as part of the standard 27-byte response. If the command is invalid, the EPS will respond with the appropriate error flag. Reasons for rejected read commands include an invalid register address or CRC.

A proper response will be structured as follows:

BYTE INDEX	BYTE NAME	BYTE MAPPING
26	DATA BYTE 15	RESERVED (0x00)
25	DATA BYTE 14	DATA BYTE
24	CRC BYTE 8	CRC BYTE 8
23-3	-	RESERVED
2	ERROR BYTE 1	ERROR BYTE 1
1	ERROR BYTE 0	ERROR BYTE 0
0	CRC BYTE 0	CRC BYTE 0

Following the response sync word, a reserved byte, the requested data byte, and then the corresponding CRC byte are transmitted by the EPS. Note that CRC BYTE 8 pertains to both the preceding reserved byte and data byte. Following CRC BYTE 8 are the two error bytes and their corresponding CRC byte.

An error bit sequence of all 0s implies that the command was executed successfully and that there are no command nor system-level errors to report. Section 12.5 outlines the error flags associated with each error bit.

12.3.6.3 Master Telemetry Bank Read Command

An 8-measurement telemetry bank is read via a Master Telemetry Bank Read Command. The first 4 bytes of the SPI command shall be structures as follows:

R/$\overline{W}$	ADDRESS BYTE						
1	A6	A6	A4	A3	A2	A1	A0

RESERVED							
0	0	0	0	0	0	0	0

CRC BYTE							
C7	C6	C5	C4	C3	C2	C1	C0

Figure 24. SPI Master Telemetry Bank Read Command Byte Structure

Upon reception of a valid read bit (R/$\overline{W}$ = 1) and register address (and reserved byte), validated via the respective CRC byte, the eight 10-bit telemetry measurements of the specified bank will be transmitted on the bus as part of the standard 27-byte response. If the command is invalid, the EPS will respond with the appropriate error flag. Reasons for rejected telemetry requests include an invalid register address or CRC.

A proper response will be structured as follows:

BYTE INDEX	BYTE NAME	BYTE MAPPING
26-25	DATA BYTE [15:14]	TELEMETRY POINT 7
24	CRC BYTE 8	CRC BYTE 8
23-22	DATA BYTE [13:12]	TELEMETRY POINT 6
21	CRC BYTE 7	CRC BYTE 7
20-19	DATA BYTE [11:10]	TELEMETRY POINT 5
18	CRC BYTE 6	CRC BYTE 6
17-16	DATA BYTE [9:8]	TELEMETRY POINT 4
15	CRC BYTE 5	CRC BYTE 5
14-13	DATA BYTE [7:6]	TELEMETRY POINT 3
12	CRC BYTE 4	CRC BYTE 4
11-10	DATA BYTE [5:4]	TELEMETRY POINT 2
9	CRC BYTE 3	CRC BYTE 3
8-7	DATA BYTE [3:2]	TELEMETRY POINT 1
6	CRC BYTE 2	CRC BYTE 2
5-4	DATA BYTE [1:0]	TELEMETRY POINT 0
3	CRC BYTE 1	CRC BYTE 1
2	ERROR BYTE 1	ERROR BYTE 1
1	ERROR BYTE 0	ERROR BYTE 0
0	CRC BYTE 0	CRC BYTE 0

Following the response sync word, eight telemetry points are transmitted by the EPS as 3-byte sets. The first two bytes of the set consist of a 10-bit telemetry value with the most significant bits (MSBs) padded as zero. The third byte in the set is the corresponding CRC byte. Following the last telemetry point set are the two error bytes and their corresponding CRC byte.

An error bit sequence of all 0s implies that the command was executed successfully and that there are no command nor system-level errors to report. Section 12.5 outlines the error flags associated with each error bit.

12.4 Cyclic Redundancy Check (CRC)

The EPS CC&DH interface employs a cyclic redundancy check (CRC) error detection scheme to enhance interface reliability and robustness. When an error is detected, the command is ignored, and the appropriate error bits are set in the response.

Each incoming CRC byte corresponds to either two or three preceding bytes depending on the interface it is transmitted over. For I2C, the CRC byte/bit alignment used by the master during CRC generation shall be:

TRANSMITTED BYTE N								TRANSMITTED BYTE N+1								TRANSMITTED BYTE N+2							
COMMAND BYTE								R/$\overline{W}$	REGISTER ADDRESS							DATA BYTE							
A6	A5	A4	A3	A2	A1	A0	R/$\overline{W}$		A6	A5	A4	A3	A2	A1	A0	D7	D6	D6	D4	D3	D2	D1	D0

TRANSMITTED BYTE N+3							
CRC BYTE							
C7	C6	C6	C4	C3	C2	C1	C0

For SPI, the CRC byte/bit alignment used by the master during CRC generation shall be:

TRANSMITTED BYTE N								TRANSMITTED BYTE N+1								TRANSMITTED BYTE N+2							
R/$\overline{W}$	REGISTER ADDRESS							DATA BYTE								CRC BYTE							
	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	C7	C6	C6	C4	C3	C2	C1	C0

Each outgoing CRC byte corresponds to the two preceding data or error bytes whether using I2C or SPI. The CRC byte/bit alignment used by the master during CRC validations shall be:

RECEIVED BYTE N								RECEIVED BYTE N+1								RECEIVED BYTE N+2							
DATA/ERROR BYTE N								DATA/ERROR BYTE N+1								CRC BYTE							
D7	D6	D6	D4	D3	D2	D1	D0	D7	D6	D6	D4	D3	D2	D1	D0	C7	C6	C6	C4	C3	C2	C1	C0

The CRC byte for both incoming and outgoing transmission strings is computed using the Baicheva generator polynomial ‘C2’:

$$x^8 + x^5 + x^3 + x^2 + x + 1. \qquad \text{Eq. 3}$$

Normal Representation: 0x2F

Additional CRC8 routine parameters are included below:

Parameter	Value
Initial Value	0xFF
Input Data Reflected?	No
Result Data Reflected?	No
Final XOR Value	0xFF

The following is example code for the generation of an 8-bit CRC value given an 8-bit input array:

```
uint8_t CRC_compute(uint8_t payload[], uint8_t payloadLength) {
      uint8_t result = CRC_INITIAL_VALUE;

      for (uint8_t b = 0; b < payloadLength; b++) {

            result ^= payload[b];

            for (uint8_t i = 0; i < 8; i++) {
                  if (result & 0b10000000) {
                        result <<= 1;
                        result ^= CRC_POLYNOMIAL;
                  }
                  else {
                        result <<= 1;
                  }
            }
      }

      return result ^ CRC_FINAL_XOR_VALUE;
}
```

12.5 Error Flags

Each response from the EPS will contain two error bytes which inform the state of the system. The SYSERRA register/byte contains flags alerting the flight computer to the occurrence of system faults.

The CCERR register/byte contains flags regarding the I2C or SPI request that it is provided as a response to.

The table below lists flag-specific information such as

- Which byte and bit maps to each flag
- Whether or not the command was executed, given the error
- And whether the flag is latching

Note: Given that these registers are provided in response to all CC&DH requests, they are not read-able stand-alone. It is recommended that a telemetry bank be read in order to obtain the state of all system error flags.

If a flag is denoted as latching, it must be cleared by writing it as a 1. See Section 12.6.6 for the relevant register details and how to clear a latching flag.

ERROR BYTE	BIT	NAME	COMMAND RESULT	NO ERROR VALUE	LATCHING?
1 (SYSERRA)	7	Battery Protection Fault	Section 12.5.1	0	Yes
	6	Battery Undervoltage Fault	Section 12.5.2	0	Yes
	5	Switched Output 4 Over-Current	Section 0	0	Yes
	4	Switched Output 3 Over-Current		0	Yes
	3	Switched Output 2 Over-Current		0	Yes
	2	Switched Output 1 Over-Current		0	Yes
	1	CC&DH WDT Timeout	Section 12.5.4	0	Yes
	0	Reserved	N/A	0	N/A
0 (CCERR)	7	Reserved	N/A	0	N/A
	6	Reserved	N/A	0	N/A
	5	Reserved	N/A	0	N/A
	4	Invalid Command	Ignored	0	No
	3	Illegal Command	Ignored	0	No
	2	CC&DH Transaction Time-Out	Note 1	0	No
	1	Consecutive CRC Error	Ignored	0	No
	0	CRC Error	Ignored	0	No

1. Command execution is dependent on how far into the transaction the time-out occurs

12.5.1 Battery Protection Fault

When the Battery Protection Fault Flag is set, the EPS has:

- Opened all switched battery power outputs

Upon clearing a Battery Protection Fault flag, the flag will be reset to 0 and all system functionality that is prevented during the existence of the flag will be permitted again. This functionality includes:

- Turning on switched outputs connected to the unregulated battery bus

Also see Section 10.

12.5.2 Battery Undervoltage Fault

When the Battery Undervoltage Fault Flag is set, the EPS has:

- Opened all switched outputs
- Disabled the 3.3-Volt converter
- Disabled the 5-Volt converter
- Defaulted all system configuration and control registers

The EPS will reenable the 5-Volt and 3.3-Volt converters autonomously when the battery undervoltage fault clears. If applicable, it will also close the dedicated CC&DH switched output.

Upon clearing a Battery Undervoltage Fault flag, the flag will be reset to 0 and all system functionality that is prevented during the existence of the flag will be permitted again. This functionality includes:

- Turning on any switched output
    - Aside from the dedicated CC&DH switched output (if applicable)

Converter disable and enable timing matches that of Section 6.3.2.

Also see Section 10.

12.5.3 Switched Output n Over-Current

When the Switched Output Over-Current Flag is set, the EPS has:

- Opened switched output 'n'

Note: These flags are latching but are not clearable via a write to the SYSERRA register. To clear these flags, see Section 12.6.3.2.

Upon clearing a Switched Output n Over-Current flag, the flag will be reset to 0 and all system functionality that is prevented during the existence of the fault will be permitted again. This functionality includes:

- Turning on switched output 'n'

Also see Section 10.

12.5.4 CC&DH WDT Timeout

When the CC&DH WDT Timeout Flag is set, the EPS has executed the appropriate external WDT reset sequence. See Section 10.7 for a detailed description of the external WDT reset behavior.

Upon clearing a CC&DH WDT Fault flag, the flag will be reset to 0. No system functionality is inhibited during the presence of this flag.

Note: This flag is not set after a global spacecraft reset.

12.6 Register Details

12.6.1 Register Summary

REGISTER ADDRESS	ACRONYM	NAME
Configuration Registers – Read/Write		
0x10	BECVCR	Battery End of Charge Voltage (EOCV) Configuration Register
0x11	MBCCCR	Maximum Battery Charge Current Configuration Register
0x12	SAVCR	Solar Array Voltage Configuration Register
0x13	-	Reserved
0x14	EWCFR	External Watchdog Configuration Register
0x15	EWRMR	External Watchdog Reset Mode Register
Control Registers – Read/Write		
0x30	EWCTR	External Watchdog Control Register
0x31	LSOCR	Latching Current Limited (LCL) Switched Outputs Control Register
0x32	NLSOCR	Non-Latching Current Limited Switched Outputs Control Register
0x33	-	Reserved
0x34	-	Reserved

REGISTER ADDRESS	ACRONYM	NAME
0x35	PPTCR	Peak Power Tracker Control Register
Telemetry Banks – Read-Only		
0x50	SVTBA	System Voltage Telemetry Bank A
0x51	-	Reserved
0x52	SCTBA	System Current Telemetry Bank A
0x53	SCTBB	System Current Telemetry Bank B
0x54	TTBA	Temperature Telemetry Bank A
0x55	-	Reserved
Status Registers – Read/Write		
0x70	SBCR	System Boot Counter Register
0x71	EWRCR	External Watchdog Reset Counter Register
0x72	-	Reserved
0x73	BPFCR	Battery Protection Fault Counter Register
Error Registers – Write-Only		
0x79	SYSERRA	System Error Register
0x7A	-	Reserved
0x7B	CCERR	Command and Control Interface Error Register
System Identification Registers – Read-Only		
0x7C	SSNR	System Serial Number Register
0x7D	SHVNR	System Hardware Version Number Register
0x7E	SSVNR	System Software Version Number Register
0x7F	-	Reserved

12.6.2 System Configuration Registers

Registers in this section begin at 0x10 and are readable and writeable via a Master Register Read Command and a Master Register Write Command, respectively.

12.6.2.1 0x10 - Battery End of Charge Voltage (EOCV) Configuration Register

BIT	NAME	DEFAULT	DESCRIPTION
7-0	EOCV Setpoint	11101001 [16.796 V]	An 8-bit value for the EOCV setpoint for the connected battery. Transfer Function: 14.00 V + (VALUE * 0.012 V)

12.6.2.2 0x11 - Maximum Battery Charge Current Configuration Register

BIT	NAME	DEFAULT	DESCRIPTION
7-0	Max Battery Charge Current	01001100 [1.470 A]	An 8-bit value for the maximum charge current for the connected battery. Transfer Function: (VALUE * 0.045149 A) – 1.961 A Min: 00000000 (equivalent to -1.961 A) Max: 10000100 (equivalent to 3.999 A)

12.6.2.3 0x12 – Solar Array Voltage Configuration Register

BIT	NAME	DEFAULT	DESCRIPTION
7-0	Fixed Solar Array Voltage	00100011 [18.966 V]	An 8-bit value for the solar array voltage setpoint. Transfer Function: (VALUE * 0.075589 V) + 16.320 V Min: 00100011 (equivalent to 18.966 V) Max: 11111111 (equivalent to 35.595 V)

12.6.2.4 [Removed]

12.6.2.5 0x14 - External Watchdog Configuration Register

BIT	NAME	DEFAULT	DESCRIPTION
7	Watchdog Enable	1	Enable/Disable external watchdog. 1 = ENABLED
6-0	Watchdog Timer Interval	1111111 [128 sec]	A 7-bit value for the external watchdog timer interval multiplier. Transfer Function: 1.0 sec + (VALUE * 1.0 sec)

1. External watchdog functionality is entirely overridden by GSE hardware signal (*I2C_WD_DIS_N*)

12.6.2.6 0x15 – External Watchdog Reset Mode Register

BIT	NAME	DEFAULT	DESCRIPTION
7-0	External Watchdog Reset Mode	00000000 [Global]	Set external watchdog timer reset mode. Write as 0x55: Non-Global Reset Default Mode: Global Reset

12.6.3 System Control Registers

Registers in this section begin at 0x30 and are readable and writeable via a Master Register Read Command and a Master Register Write Command, respectively.

12.6.3.1 0x30 - External Watchdog Control Register

BIT	NAME	DEFAULT	DESCRIPTION
7-1	Reserved	0	Reserved. Write as 0.
0	Pet Bit	0	Write as 1 to reset watchdog timer. Self-clearing. Note 2,3

1. External watchdog functionality is entirely overridden by GSE hardware signal (*I2C_WD_DIS_N*)
2. Writing Pet Bit as 0 will return an Illegal Command flag
3. If the pet is unsuccessful, an Illegal Command flag will be returned

12.6.3.2 0x31 – Latching Current Limited (LCL) Switched Outputs Control Register

BIT	NAME	DEFAULT	DESCRIPTION
7	LCL 4 Trip Indicator	0 (Note 1)	LCL trip indicator for switch 4. 1 = TRIPPED
6	LCL 3 Trip Indicator	0 (Note 1)	LCL trip indicator for switch 3. 1 = TRIPPED
5	LCL 2 Trip Indicator	0 (Note 1)	LCL trip indicator for switch 2. 1 = TRIPPED
4	LCL 1 Trip Indicator	0 (Note 1)	LCL trip indicator for switch 1. 1 = TRIPPED
3	Switch 4 State	0	Write as 1 to energize switched output 4.

BIT	NAME	DEFAULT	DESCRIPTION
2	Switch 3 State	0	Write as 1 to energize switched output 3.
1	Switch 2 State	0	Write as 1 to energize switched output 2.
0	Switch 1 State	0	Write as 1 to energize switched output 1.

1. After a trip, LCL Trip Indicator bit(s) must be written as a 1 before respective switch(es) can be commanded closed. If a switch trip indicator bit is written as a 1 at the same time as the respective switch state bit, the switch will be closed.

12.6.3.3 0x32 – Non-Latching Current Limited Switched Outputs Control Register

BIT	NAME	DEFAULT	DESCRIPTION
7	Reserved	0	Reserved. Write as 0.
6	Reserved	0	Reserved. Write as 0.
5	Switch10 State	0	Write as 1 to energize switched output 10. For battery heater only.
4	Switch 9 State	0	Write as 1 to energize switched output 9. For battery heater only.
3	Switch 8 State	0	Write as 1 to energize switched output 8.
2	Switch 7 State	0	Write as 1 to energize switched output 7.
1	Switch 6 State	0	Write as 1 to energize switched output 6.
0	Switch 5 State	0	Write as 1 to energize switched output 5.

12.6.3.4 0x35 – Peak Power Tracker Control Register

BIT	NAME	DEFAULT	DESCRIPTION
7-1	Reserved	0	Reserved. Write as 0.
0	PPT Enable Bit	0	Write as 1 to enable peak power tracking functionality.

12.6.4 System Telemetry Banks

Telemetry banks in this section begin at 0x50 and are read-only. All telemetry in a bank is read via a Master Telemetry Bank Read Command. Each 10-bit value is represented across 2 data bytes as specified in the following tables.

12.6.4.1 0x50 – System Voltage Telemetry Bank A

DATA BYTE	BIT	NAME
15	7-2	Reserved
	1-0	Solar Array Voltage [9-8]
14	7-0	Solar Array Voltage [7-0]
13	7-2	Reserved
	1-0	Battery Bus Voltage [9-8]
12	7-0	Battery Bus Voltage [7-0]
11	7-2	Reserved
	1-0	5V Converter Output Voltage [9-8]
10	7-0	5V Converter Output Voltage [7-0]
9	7-2	Reserved
	1-0	12V Converter Output Voltage [9-8]
8	7-0	12V Converter Output Voltage [7-0]

DATA BYTE	BIT	NAME
7	7-2	Reserved
	1-0	3.3V Housekeeping Voltage [9-8]
6	7-0	3.3V Housekeeping Voltage Bits [7-0]
5	7-2	Reserved
	1-0	12V Housekeeping Voltage [9-8]
4	7-0	12V Housekeeping Voltage [7-0]
3	7-2	Reserved
	1-0	30V Housekeeping Voltage [9-8]
2	7-0	30V Housekeeping Voltage [7-0]
1	7-2	Reserved
	1-0	3.3V Converter Output Voltage [9-8]
0	7-0	3.3V Converter Output Voltage [7-0]

12.6.4.2 0x51 – Reserved

Reserved for future expansion.

12.6.4.3 0x52 – System Current Telemetry Bank A

DATA BYTE	BIT	NAME
15	7-2	Reserved
	1-0	Solar Array Current [9-8]
14	7-0	Solar Array Current [7-0]
13	7-2	Reserved
	1-0	Battery Charge Current [9-8]
12	7-0	Battery Charge Current [7-0]
11	7-2	Reserved
	1-0	5V Converter Output Current [9-8]
10	7-0	5V Converter Output Current [7-0]
9	7-2	Reserved
	1-0	12V Converter Output Current [9-8]
8	7-0	12V Converter Output Current [7-0]
7	7-2	Reserved
	1-0	Switched Output 1 Current [9-8]
6	7-0	Switched Output 1 Current [7-0]
5	7-2	Reserved
	1-0	Switched Output 2 Current [9-8]
4	7-0	Switched Output 2 Current [7-0]
3	7-2	Reserved
	1-0	Switched Output 3 Current [9-8]
2	7-0	Switched Output 3 Current [7-0]
1	7-2	Reserved
	1-0	Switched Output 4 Current [9-8]
0	7-0	Switched Output 4 Current [7-0]

12.6.4.4 0x53 – System Current Telemetry Bank B

DATA BYTE	BIT	NAME
15	7-2	Reserved

DATA BYTE	BIT	NAME
	1-0	Battery Discharge Current [9-8]
14	7-0	Battery Discharge Current [7-0]
13	7-2	Reserved
	1-0	3.3V Converter Output Current [9-8]
12	7-0	3.3V Converter Output Current [7-0]
11-0	7-0	Reserved

12.6.4.5 0x53 – Reserved

Reserved for future expansion.

12.6.4.6 0x54 – Temperature Telemetry Bank A

DATA BYTE	BIT	NAME
15	7-2	Reserved
	1-0	System Temperature [9-8]
14	7-0	System Temperature [7-0]
13	7-2	Reserved
	1-0	Solar Array Temperature B [9-8] (THRM4)
12	7-0	Solar Array Temperature B [7-0] (THRM4)
11	7-2	Reserved
	1-0	Solar Array Temperature A [9-8] (THRM3)
10	7-0	Solar Array Temperature A [7-0] (THRM3)
9	7-2	Reserved
	1-0	Battery Temperature B [9-8] (THRM2)
8	7-0	Battery Temperature B [7-0] (THRM2)
7	7-2	Reserved
	1-0	Battery Temperature A [9-8] (THRM1)
6	7-0	Battery Temperature A [7-0] (THRM1)
5-0	7-0	Reserved

12.6.4.7 0x55 – Reserved

Reserved for future expansion.

12.6.5 System Status Registers

Registers in this section begin at 0x70 and are readable and writeable via a Master Register Read Command and a Master Register Write Command, respectively.

12.6.5.1 0x70 – System Boot Counter Register

BIT	NAME	DEFAULT	DESCRIPTION
7-0	System Boot Count	N/A	The number of times that the system has booted since the last time the register was written. Writing this register with any data byte will reset it to 0x00.

12.6.5.2 0x71 - External Watchdog Reset Counter Register

BIT	NAME	DEFAULT	DESCRIPTION
7-0	External Watchdog Reset Count	N/A	The number of times that the external watchdog has timed-out and power cycled the spacecraft since the last time the register was written. See Section 10.7 for a detailed description of the external watchdog functionality. Writing this register with any data byte will reset it to 0x00.

12.6.5.3 0x73 – Battery Protection Fault Counter Register

BIT	NAME	DEFAULT	DESCRIPTION
7-0	Battery Protection Fault Quantity Count	N/A	The number of times that the high-side battery protection trips. Specifically, this counter is incremented when the battery is protected due to either a battery over-current (charge) fault or an over-voltage fault. See Section 10.2.1 for a description of this fault scenario. Writing this register with any data byte will reset it to 0x00.

See Section 15.1 for additional details regarding this register.

12.6.6 Error Registers

Registers in this section begin at 0x79 and are writeable via a Master Register Write Command.

Note: Not all bits in these registers are writeable. Writeable bits are called-out in the following sub-sections. Writing a 1 to a set, latched flag will reset it to 0. Writing 0 to a latched or non-latched flag has not effect.

An "Illegal Command" response resulting from a write to a register in this section signifies that the fault for which the flag clearing attempt was made is still present. If this occurs, the flag will not be cleared and a re-attempt will have to be made at a later date.

12.6.6.1 0x79 – System Error Register

BIT	NAME	DESCRIPTION
7	Battery Protection Fault	Write as 1 to acknowledge fault, restore inhibited functionality, and clear error flag.
6	Battery Undervoltage Fault	Write as 1 to acknowledge fault, restore inhibited functionality, and clear error flag.
5	Switched Output 4 Over-Current	Cleared via a write to LSOCR. Section 12.6.3.2.
4	Switched Output 3 Over-Current	Cleared via a write to LSOCR. Section 12.6.3.2.
3	Switched Output 2 Over-Current	Cleared via a write to LSOCR. Section 12.6.3.2.
2	Switched Output 1 Over-Current	Cleared via a write to LSOCR. Section 12.6.3.2.
1	C&DH WDT Timeout	Write as 1 to acknowledge fault and clear error flag.
0	Reserved	Reserved

12.6.6.2 0x7B – Command and Control Interface Error Register

There are no flags in this register that are latching. Flags are generated on a request-by-request basis. Writes to this register will result in an "Invalid Command" response.

12.6.7 System Identification Registers

Registers in this section begin at 0x7C and are readable via a Master Register Read Command. Registers in this section are read-only.

12.6.7.1 0x7C – System Serial Number Register

BIT	NAME	DEFAULT	DESCRIPTION
7-0	System Serial Number	N/A	The unique serial number for the unit being commanded.

12.6.7.2 0x7D – System Hardware Version Number Register

BIT	NAME	DEFAULT	DESCRIPTION
7-4	Major Hardware Version Number	N/A	The major hardware configuration version number of the unit being commanded.
3-0	Minor Hardware Version Number	N/A	The minor hardware configuration version number of the unit being commanded.

12.6.7.3 0x7E – System Software Version Number Register

BIT	NAME	DEFAULT	DESCRIPTION
7-4	Major Software Version Number	N/A	The major version number of the software installed on the unit being commanded.
3-0	Minor Software Version Number	N/A	The minor version number of the software installed on the unit being commanded.

13 MECHANICAL/THERMAL INTERFACE

The EPS card is designed to accommodate several mounting interfaces including:

1. With installed card-mounted wedge locks into a thermally conductive, electrically grounded chassis.
2. With chassis-mounted card-locks in a thermally conductive, electrically grounded chassis.
3. With a bolted interface to a thermally conductive, electrically grounded chassis. A thermal interface material is recommended for this configuration to minimize the interface temperature rise.

Heat is conducted through the edges of the EPS circuit card via the side of the PCB opposite the wedge locks or bolted interface. It is important that the fasteners or wedge locks are installed correctly and torqued to the manufacturer recommended pressure.

Note: Wedge locks are not installed as part of the as-delivered EPS assembly and are the responsibility of the user to install correctly on both the EPS card as well as the chassis in which the EPS card is mounted.

13.1 Thermal Considerations.

The EPS card is designed to operate with a maximum thermal interface temperature of 60C. Testing has been performed at maximum power and with converters taken to foldback levels at this temperature to ensure that the unit can operate reliably when within its recommended limits over a full mission duration. It is of high importance that the thermal resistance between the EPS board and the mounting interface is minimized to prevent thermal overstress.

There may be thermal interface temperatures above 61C at which components could go into thermal runaway modes when operating at foldback or maximum rated levels due to the dissipation of a component increasing with high temperature.

Ibeos should be consulted prior to operating the EPS above 100W total input power with interface temperatures above 61C. If testing above that temperature and power is performed, it is recommended to telemeter key component temperatures during ground testing to verify that the spacecraft configuration provides adequate thermal margins for long-term reliability.

14 SYSTEM TESTING

Testing of the EPS shall be in accordance with the *EPS Test Procedure* document. Testing includes a full functional test at ambient, hot, and cold conditions including both hot and cold-start. Hot testing is performed with a 60C interface temperature; cold testing is performed with a -35C interface temperature.

Typical acceptance testing includes 9 hot and 8 cold plateaus with functional tests performed at the first and last hot and cold plateaus. The first plateau is hot 1; the last is hot 9. During cycles hot 2 through hot 8 (encompassing cold 2 through 7), the EPS card is operated in monitor mode.

Monitor mode is a static configuration with each switched output closed and loaded such that the following approximate loads are applied to each power converter:

3.3V Converter:	10W
5V Converter:	30W (20W on 5V outputs, 10W from 3.3V converter load)
12V Converter:	36W

Additionally, the battery interface is commanded to change at 1A, and the battery bus is loaded with approximately 4A. This results in a total solar array interface input power of approximately 150W.

In addition to thermal cycles, the EPS card undergoes burn-in testing at a 60C interface temperature to reach a total operating time (including thermal cycles and functional tests) of 200 hours. Burn-in testing is performed in monitor mode.

15 ERRATA

15.1 Battery Protection Fault Counter

The EPS battery protection counter that is implemented inside of the EPS MCU (Section 12.6.5.3) will increment its count each time the 3.3-Volt housekeeping supply drops out of regulation. The following events result in this behavior:

- Internal watchdog timer reset
- External watchdog timer reset (global reset mode only)
- Entering eclipse/shadow while in battery undervoltage
- Closing the inhibits from an open state (terrestrial use only)

16 APPENDIX A: HARDWARE CONFIGURABLE PARAMETERS

Several parameters of the EPS unit may be configured during manufacture by modifying part values and/or jumpers. This specification provides the performance with the standard (default) configuration. Alternate configurations must be specified at time of order and may have additional cost/lead time. Hardware configuration should not be modified except by Ibeos.

Jumper 1 (J4): Switch 1 output is selectable between 3.3V regulated, 5V regulated, and 12V regulated, unregulated battery voltage.

Jumper 2 (J5): Switch 2 output is selectable between 3.3V regulated, 5V regulated, and 12V regulated, unregulated battery voltage.

Jumper 3 (J6): Switch 3 output is selectable between 3.3V regulated, 5V regulated, and 12V regulated, unregulated battery voltage.

Jumper 4 (J7): Switch 4 output is selectable between 3.3V regulated, 5V regulated, and 12V regulated, unregulated battery voltage.

Jumper 5 (J8): Switch 5 output is selectable between 3.3V regulated, 5V regulated, and 12V regulated, unregulated battery voltage.

Jumper 6 (J6): Switch 6 output is selectable between 3.3V regulated, 5V regulated, and 12V regulated, unregulated battery voltage.

Jumper 7 (J7): Switch 7 output is selectable between 3.3V regulated, 5V regulated, and 12V regulated, unregulated battery voltage.

Jumper 8 (J8): Switch 8 output is selectable between 3.3V regulated, 5V regulated, and 12V regulated, unregulated battery voltage.

Battery Overvoltage may be adjusted for higher or lower trip points.

Battery Overcharge Current may be adjusted for lower trip points.

Battery Undervoltage may be adjusted for lower trip points.

Battery Overdischarge Current may be adjusted for lower trip points.

17 APPENDIX B: SOFTWARE CONFIGURABLE PARAMETERS

These parameters are hardcoded in the EPS MCU software. This specification provides the performance of the standard (default) configuration. Alternate configurations must be specified at time of order and may have additional cost/lead time. Software configuration should not be modified except by Ibeos.

Parameter	Default/Reset Value	CC&DH Commandable?
Default Maximum Charge Current	See Section 12.6.2.2	Yes
Default Battery End of Charge Voltage	See Section 12.6.2.1	Yes
Default Solar Array Voltage Set-Point	See Section 12.6.2.3	Yes
Default Solar Array Minimum Voltage	See Section 7.2	No
Switch 1 Overcurrent Limit	See Section 5.4.5	No
Switch 2 Overcurrent Limit		No
Switch 3 Overcurrent Limit		No
Switch 4 Overcurrent Limit		No
Default CC&DH Watchdog Timeout	See Section 12.6.2.5	Yes
Default CC&DH Watchdog Enable	See Section 12.6.2.5	Yes

18 APPENDIX C: REFERENCE TEST DATA

The figures in this section are intended to show typical operation of the EPS assembly and are intended for reference. Measurements are at beginning of life at 25°C, unless otherwise stated. They are not intended as bounding or worst-case limits.

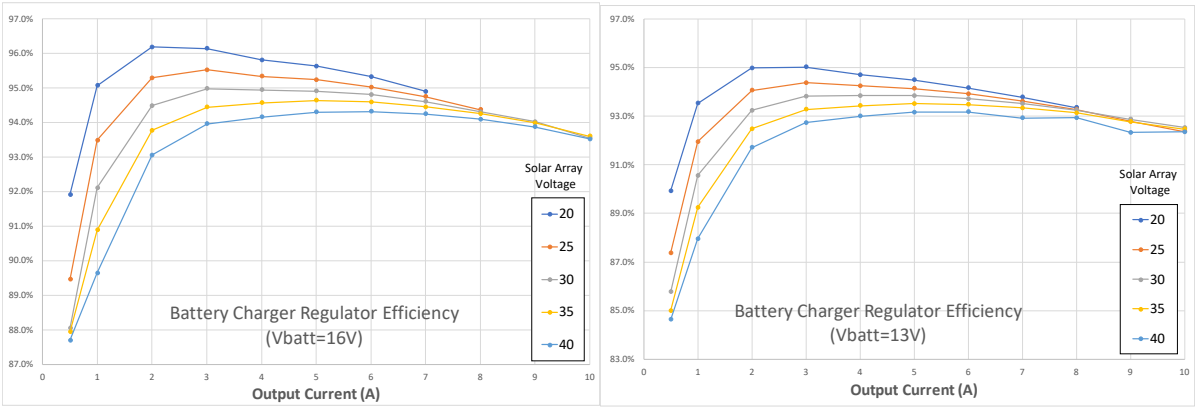


Figure 25. Battery Charge Regulator Efficiency

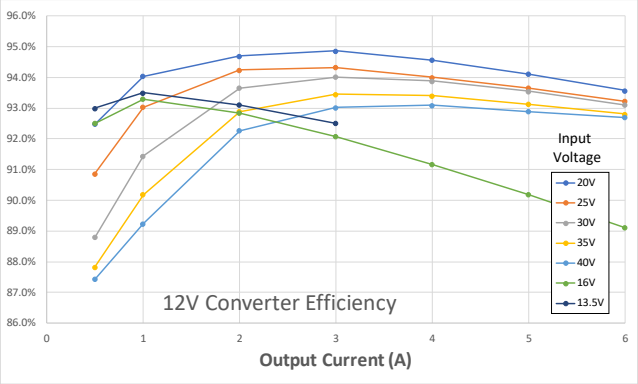


Figure 26. 12V Converter Efficiency [TBR]

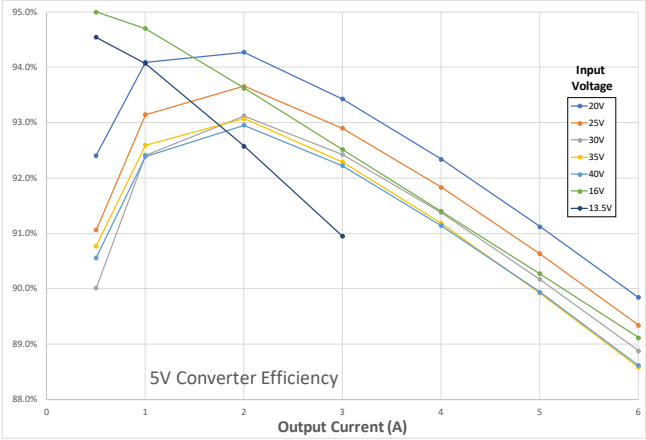


Figure 27. 5V Converter Efficiency

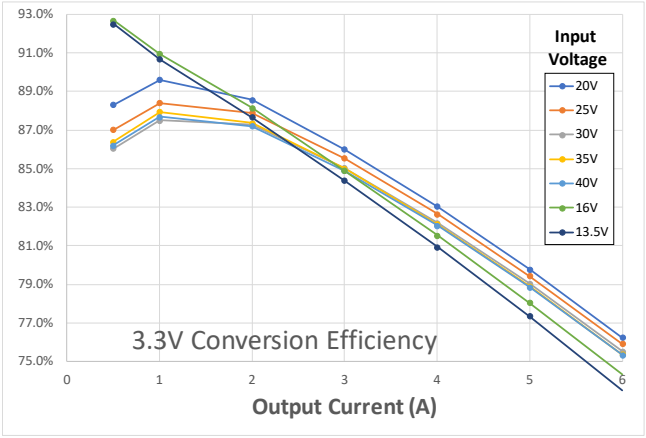


Figure 28. 3.3V Conversion Efficiency (includes 5V converter losses) [TBR]

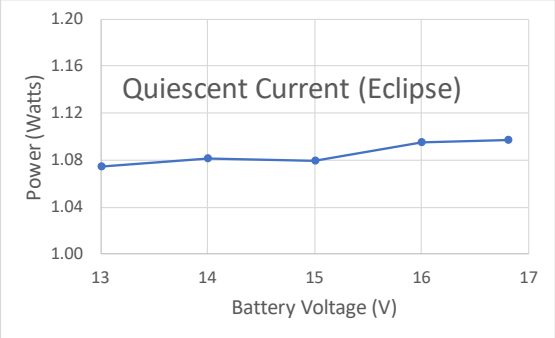


Figure 29. Quiescent Current (Eclipse) [TBR]

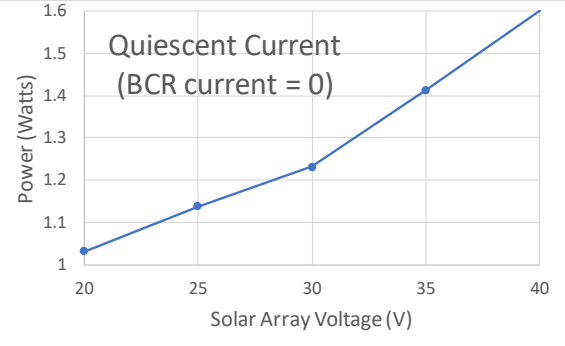


Figure 30. Quiescent Current (BCR Iout=0A) [TBR]

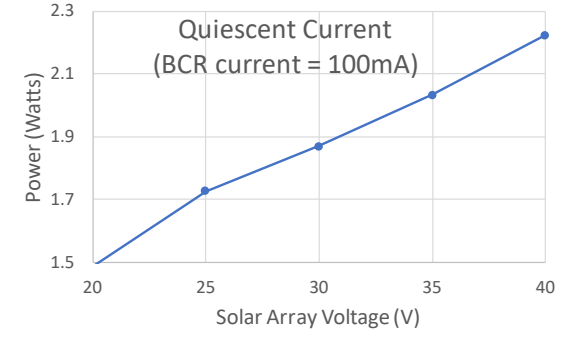


Figure 31. Quiescent Current (BCR Iout=100mA) [TBR]